DESCRIPTION

The ES1868 *Audio***Drive**® is a single, mixed-signal digital audio chip that can be designed into a motherboard, add-in card, or integrated into other peripheral cards to provide stereo sound and FM music synthesis to personal computers. The ES1868 can record, compress, and play back voice, sound, and music using built-in mixer controls. It also supports Plug and Play (PnP) standard and provides Plug and Play configuration for the following logical devices: CD-ROM (IDE), Modem, and a general-purpose I/O device.

The ES1868 contains an embedded microprocessor, 20-voice **ESFM**™ music synthesizer, 16-bit stereo wave ADC and DAC, 16-bit stereo music DAC, MPU-401 serial port, dual game ports, two serial interfaces to external DSP and external wavetable music synthesizer, DMA control logic with FIFO, ISA bus interface logic, and hardware master volume control. An internal preamp accepts 3 stereo inputs and a mono microphone input.

The Advanced Power Management (APM) features include suspend/resume from disk or host-independent, self-timed power-down and automatic wake-up.

A DSP serial interface allows an external DSP to take over resources such as ADC or DACs. Control of I/O address, DMA, and interrupt selection can be by jumper or through system software.

The UART Mode of the MPU-401 serial port enables interfacing to MIDI devices, wavetable synthesizers, and an external MIDI serial port. The dual game ports support two joysticks with X, Y resistor value settings and two pushbutton switches.

The ES1868 is compatible with Sound Blaster™; Sound Blaster™ Pro version 3.01, voice and music functions; and OPL3™ FM synthesizers. The **ESFM**™ synthesizer is register compatible with the OPL3 and has extended capabilities in native mode that provide superior sound and advanced power-down capabilities.

FEATURE HIGHLIGHTS

- High-performance, mixed-signal, 16-bit stereo VLSI chip
- High-quality, 20-voice **ESFM**™ music synthesizer; patents pending
- Patented **ESPCM**® compression
- CD-ROM IDE Interface
- High-performance DMA supports demand transfer and F-type DMA

Plug and Play (PnP) Features

- On-chip PnP support for audio, joystick port, FM, modem, MPU-401, CD-ROM, and user-defined I/O
- Software address mapping, and four DMA and six IRQ selections for motherboard implementation
- Internal masked ROM support for PnP configuration resource
- Ability to write unique ID numbers on each board by programming the external EEPROM through the ES1868

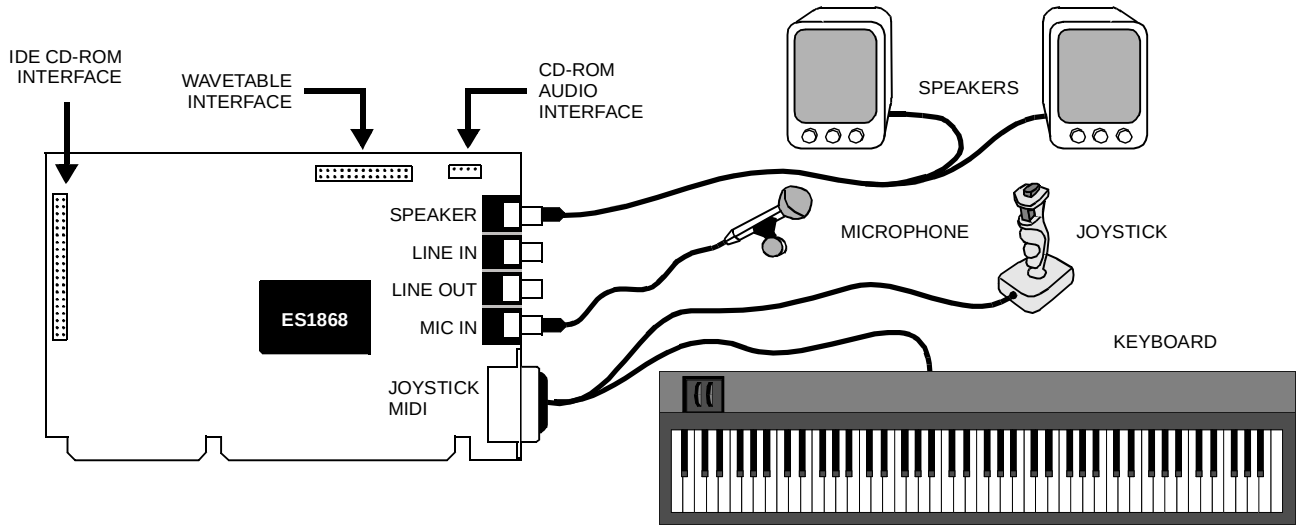

Figure 1 ES1868 Sound Card Application

Record and Playback Features

- Record, compress, and play back voice, sound, and music
- 16-bit stereo ADC and DAC
- Programmable sample rates from 4 kHz to 44.1 kHz for record and playback
- Full-duplex monophonic mode, half-duplex stereo mode
- 6-bit (64 step) master volume control
- 3-button hardware volume control for up, down, and mute

Inputs/Outputs

- Stereo inputs for line-in, CD-ROM, and AUX, and a mono input for microphone
- MPU-401 (UART Mode) interface for wavetable synthesizers and MIDI devices
- Integrated dual game ports
- Serial port interface to external DSP optionally controls full-duplex operation
- Read/write serial interface for PnP EEPROM

Mixer Features

- 6-channel stereo mixer with stereo for line, CD audio, TV, music, and digitized audio, and mono for microphone
- Mixer-controlled record and playback with logarithmic volume controls

Power

- Advanced power management with self-timed power-down, automatic wake-up, and suspend/resume
- Supports 3.3 V or 5.0 V operation

Compatibility

- Supports PC games and applications for Sound Blaster, Sound Blaster Pro, and OPL3 FM synthesizers

Operating Systems

- Microsoft Windows®95
- Microsoft Windows™ 3.1 and Windows for Workgroups™
- Windows Sound System®
- Microsoft Windows NT™ 3.51 & 4.0
- IBM® OS/2® Warp™

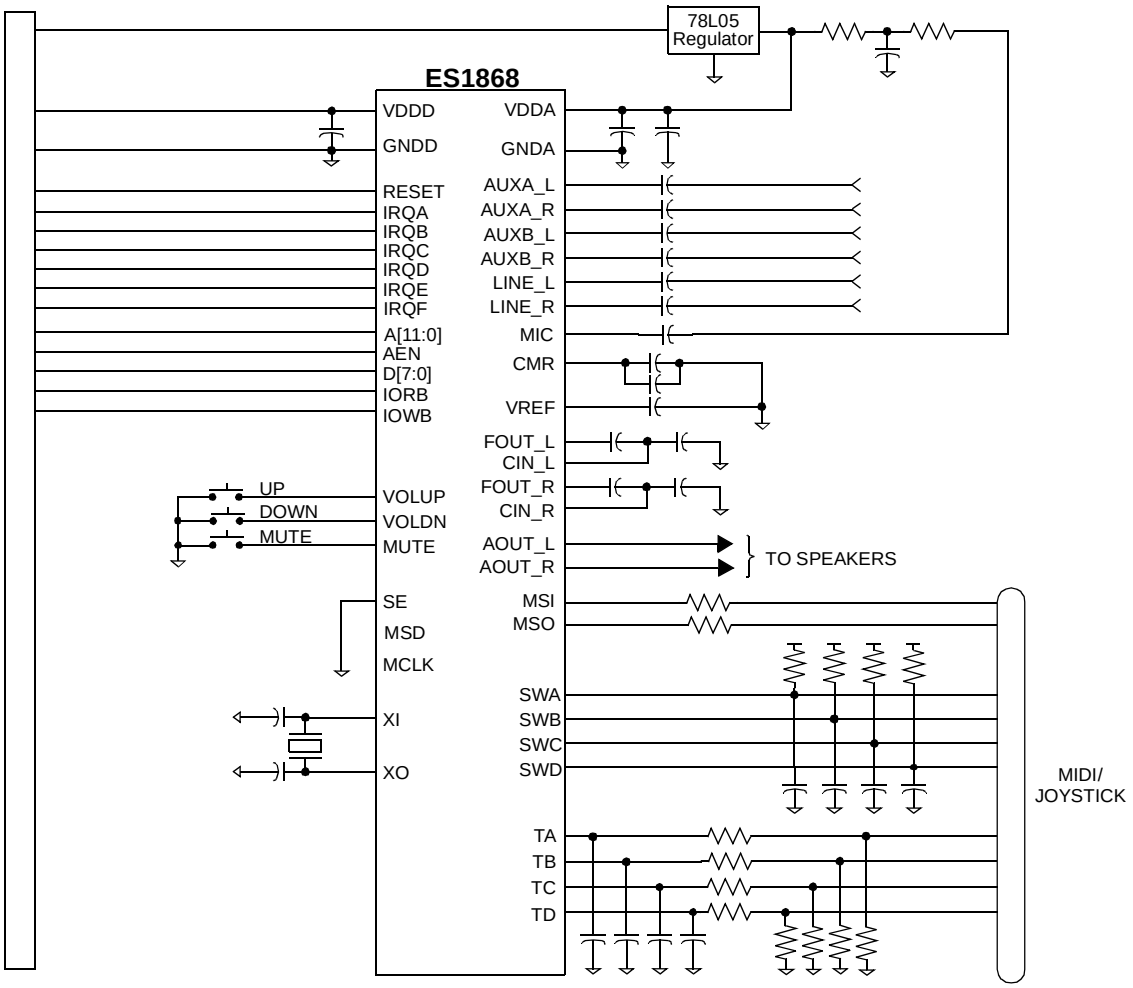

Figure 2 Typical Application

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Revision History

REV	Changes
A	Initial document.
B	Addition of Appendix C, reformatting of pin descriptions, changing of address and logo to specifications.

CONTENTS

FIGURES

TABLES

PINOUT DIAGRAM

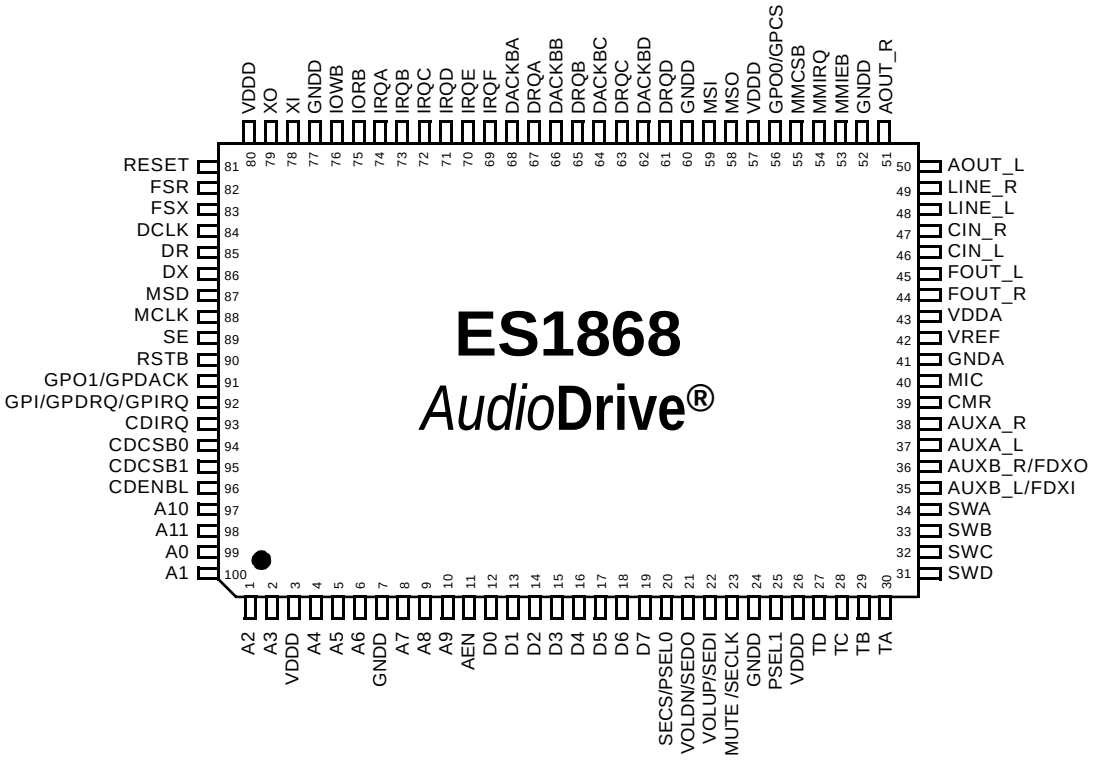


Figure 3 ES1868 Pinout

PIN DESCRIPTIONS

Table 1 Analog Pins

Name	Number	I/O	Description
Power and Ground			
VDDA	43	I	Analog supply voltage (4.5V to 5.5V). Must be greater than or equal to VDDD-0.3V.
GNDA	41	I	Analog ground.
Recording Source and Input Volume Control			
LINE_L	48	I	Line input left. LINE_L has internal pull-up resistors to the CMR pin.
LINE_R	49	I	Line input right. LINE_R has internal pull-up resistors to CMR.
AUXA_L	37	I	Auxiliary input left. AUXA_L has internal pull-up resistors to CMR. Normally intended for connection to an internal or external CD-ROM analog output.
AUXA_R	38	I	Auxiliary input right. AUXA_R has internal pull-up resistors to CMR. Normally intended for connection to an internal or external CD-ROM analog output.
AUXB_L *	35	I	Multipurpose pin. AUXB_L (Aux B input left) or FDXI.When used AUXB_L, has internal pull-up resistors to CMR. Normally intended for connection to an external music synthesizer or other line-level source.
AUXB_R *	36	I	Multipurpose pin. AUXB_R (Aux B input right) or FDXO. When used as AUXB_R, has internal pull-up resistors to CMR. Normally intended for connection to an external music synthesizer or other line-level source.
MIC	40	I	Microphone input. MIC has an internal pull-up resistor to CMR.

Table 1 Analog Pins

Name	Number	I/O	Description
Output Volume Control and Record Monitor			
AOUT_L	50	O	Analog output left from master volume.
AOUT_R	51	O	Analog output right from master volume.
DSP Interface			
FDXI *	35	I	Multipurpose pin. AUXB_L or FDXI. When used as FDXI, is input with internal pull-up to CMR. Alternate input to left channel filter stage in DSP serial mode.
FDXO *	36	O	Multipurpose pin. AUXB_R or FDXO. When used as FDXO, is normally connected to CMR via an internal resistor. Can be programmed to connect internal to FOUT_R pin during DSP serial mode.
Miscellaneous Analog Pins			
CIN_L	46	I	Capacitive coupled input left. Has internal pull-up resistor to CMR of approximately 50k ohms.
CIN _R	47	I	Capacitive coupled input right. Has internal pull-up resistor to CMR of approximately 50k ohms.
FOUT_L	45	O	Filter output left. AC-coupled externally to CIN_L to remove DC offsets. Has internal series resistor of about 5k ohms. Capacitor to analog ground on this pin can be used to create a low-pass filter pole that removes switching noise introduced by the switched-capacitor filter.
FOUT_R	44	O	Filter output right. AC-coupled externally to CIN_R to remove DC offsets. Has internal series resistor of about 5k ohms. Capacitor to analog ground on this pin can be used to create a low-pass filter pole that removes switching noise introduced by the switched-capacitor filter.
CMR	39	O	Buffered reference output. Should be bypassed to analog ground with a 47 µf electrolytic capacitor with a 0.1 µf capacitor in parallel.
VREF	42	O	Reference generator resistor divider output. Should be bypassed to analog ground with 0.1 µf capacitor.

* These pins are shared with other functions.

Table 2 Digital Pins

Name	Number	I/O	Description
Power and Ground			
VDDD	3, 26, 57, 80	I	Digital supply voltage (3.0 V to 5.5 V).
GNDD	7, 24, 52, 60, 77	I	Digital ground.
ISA Bus Interface			
A[11:10]	98:97	I	Address inputs from ISA bus. The ES1868 requires these pins to be low for all address decodes.
A[9:0]	10:8, 6:4, 2:1, 100:99	I	ISA bus address inputs.
AEN	11	I	ISA active-low address enable.
D[7:0]	19:12	I/O	ISA Bidirectional data bus. These pins have weak pull-up devices to prevent these inputs from floating when not driven.
IORB	75	I	ISA active-low read strobe.
IOWB	76	I	ISA active-low write strobe.
IRQ(A-F)	74:69	O	Six (A, B, C, D, E, F) active-high interrupt requests to the ISA bus. Unselected IRQ outputs are high-impedance. IRQs are software configurable.
DRQ(A-D)	67, 65, 63, 61	O	Four (A, B, C, D) active-high DMA requests to the ISA bus. Unselected DRQ outputs are high-impedance. When DMA is not active, the selected DRQ output has a pull-down device that holds the DRQ line inactive unless another device that shares the same DRQ line can source enough current to make the DRQ line active. DRQs are software configurable.
DACKB(A-D)	68, 66, 64, 62	I	Four (A, B, C, D) active-low DMA acknowledge inputs.
RESET	81	I	Active-high. Reset from ISA bus.
RSTB	90	O	Inverted RESET output.

Table 2 Digital Pins

Name	Number	I/O	Description
MPU-401 Serial Port (MIDI) and FIFOS			
MSO	58	O	MIDI serial data output.
MSI	59	I	MIDI serial data input. Schmitt trigger input with internal pull-up resistor. Either MPU-401 or Sound Blaster formats.
Dual Game Port Joystick			
SW(A-D)	31, 32, 33, 34	I	Active-low. Joystick switch setting inputs. These SW pins have an internal 2k ohm pull-up resistor. The joystick port is typically at address 201.
T(A-D)	30:27	I/O	Joystick timer pins. These pins connect to the X-Y positioning variable resistors for the two joysticks.
ES689/ES690 Wavetable Interface			
MSD	87	I	Input with internal pull-down. Music serial data from external ES689 or ES690 music synthesizer.
MCLK	88	I	Input with internal pull-down. Music serial clock from external ES689 or ES690 music synthesizer.
DSP/CODEC Interface			
FSR	82	I	Input with internal pull-down. Frame sync for receive data from external DSP. Programmable for active-high or active-low.
FSX	83	I	Input with internal pull-down. Frame sync for transmit request from external DSP. Programmable for active-high or active-low.
DCLK	84	I	Input with internal pull-down. Serial data clock from external DSP. Typically 2.048 MHz.
DR	85	I	Input with internal pull-down. Data receive pin from external DSP.
DX	86	O	Tri-state output. Data transmit to external DSP. High-impedance when not transmitting.
SE	89	I	Input with internal pull-down. Active high to enable serial mode, that is, enables an external DSP to control analog resources of the ES1868 through the DSP serial interface.
External Hardware Volume Control			
VOLDN *	21	I	Multipurpose pin. VOLDN or SEDO. When used as VOLDN, is an active-low, volume decrease button input.
VOLUP *	22	I	Multipurpose pin. VOLUP or SEDI. When used as VOLUP, is an active-low, volume increase button input.
MUTE *	23	I	Multipurpose pin. MUTE or SECLK. When used as MUTE, is an active-low, mute toggle button input.
CD-ROM/PnP I/O Interface			
CDIRQ	93	I	The interrupt request input from the CD-ROM.
CDCSB0	94	O	CD-ROM CS 0 pin.
CDCSB1	95	O	CD-ROM CS 1 pin.
CDENBL	96	O	CD-ROM enable pin.
EEPROM/PnP I/O Interface			
SEDO *	21	I	Multipurpose pin. VOLDN or SEDO. When used as SEDO, is an input connected to the data output pin of external PnP serial EEPROM.
SEDI *	22	I	Multipurpose pin. VOLUP or SEDI. When used as SEDI, is an input connected to data output pin from external PnP serial EEPROM.
SECLK *	23	O	Multipurpose pin. MUTE or SECLK. When used as SECLK, provides clock to external serial EEPROM clock pin for PnP.
SECS *	20	I/O	Multipurpose pin. SECS or PSEL0. When used as SECS, is a serial EEPROM CS. This is an input pin during reset.
PSEL0 *	20	I	Multipurpose pin. SECS or PSEL0. When used as PSEL0, select the PnP ROM device used along with PSEL1.

Table 2 Digital Pins

Name	Number	I/O	Description
PSEL1	25	I	Provides the following functions when used together with pin 20 when that pin is in PSEL0 mode: **PSEL1** **SECS/PSEL0** **Function** 0 0 Internal ROM 1 1 93LC66 – 512 x 8, 9 address bits
Modem/PnP I/O Interface			
MMCSB	55	O	Output from ES1868 for the Modem CSB. The address space is determined by the PnP configuration.
MMIRQ	54	I	IRQ input from the Modem device that gets mapped to an IRQ output on the ES1868 based on the PnP configuration.
MMIEB	53	I	Modem interrupt enable input. Generated from the Modem UART.
General-Purpose/PnP I/O Interface			
GPO0 *	56	O	Multipurpose pin. GPO0 or GPCS. When used as GPO0, is an output that is set low by external reset and thereafter is controlled by bit 0 of port 2x7h. Available to system software for power management or other applications.
GPCS *	56	O	Multipurpose pin. GPO0 or GPCS. When used as GPCS, if selected by the PnP logic, is a user-defined general-purpose CS, based on the PnP configuration.
GPO1 *	91	O	Multipurpose pin. GPO1 or GPDACK. When used as GPO1, is an output that is set high by external reset and thereafter controlled by bit 1 of port 2x7h. Available to system software for power management or other applications.
GPDACK *	91	O	Multipurpose pin. GPO1 or GPDACK. When used as GPDACK, can be used as a DMA channel DACK for the Modem, CD-ROM, or the user-defined general-purpose device.
GPI *	92	I	Multipurpose pin. GPI, GPDRQ, or GPIRQ. When used as GPI, is a general-purpose input pin.
GPDRQ *	92	I	Multipurpose pin. GPI, GPDRQ or GPIRQ. When used as GPDRQ, this is a DMA request output from the Modem, CD-ROM, or the user-defined device based on the PnP configuration.
GPIRQ *	92	I	Multipurpose pin. GPI, GPDRQ or GPIRQ. When used as GPIRQ,this is an IRQ output from the CD-ROM or the user-defined device based on the PnP configuration.
Miscellaneous Digital Pins			
XI	78	I	Crystal oscillator input.
XO	79	O	Crystal oscillator output.

* These pins are shared with other functions.

FUNCTIONAL DESCRIPTION

This section shows the overall structure of the ES1868 and discusses its major functional subunits.

Block Diagram

The major subsystems of the ES1868 are shown in Figure 4 and described briefly in the following bulleted lists.

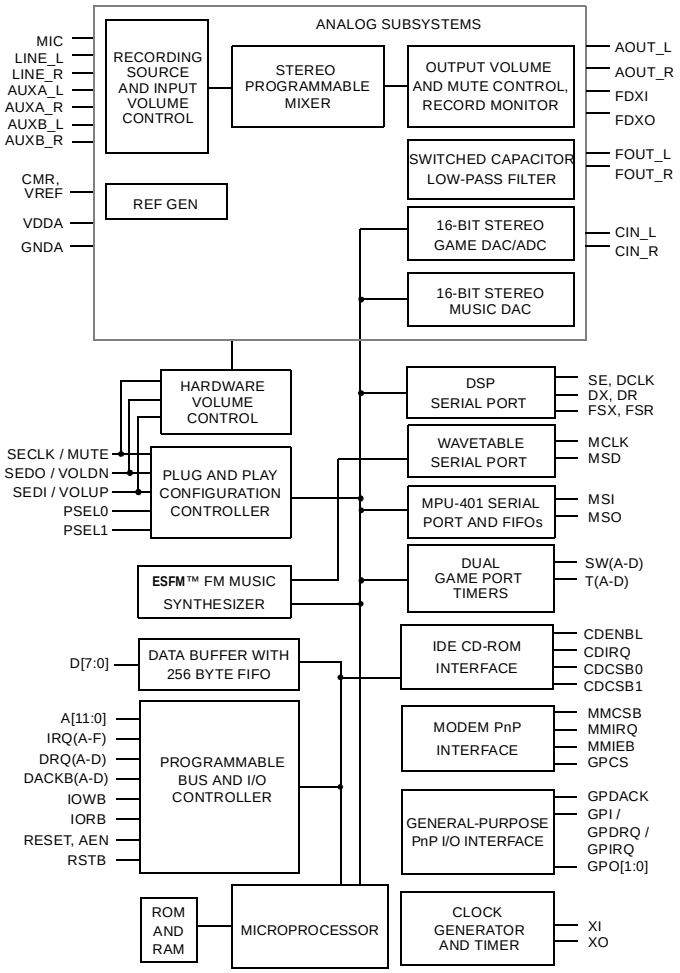


Figure 4 ES1868 Block Diagram

Digital Subsystems

- **Microprocessor** – data management and system control is performed by an embedded microprocessor.
- **Clock generator and timer** – circuitry to support an external crystal oscillator.
- **ROM and RAM** – firmware ROM and data RAM to the embedded processor.
- **Data Buffer with 256-byte FIFO** – RAM for a 256-byte FIFO data buffer.
- **Programmable bus and I/O controller** – ISA bus interface.
- **Plug and Play configuration controller** – provides the following features:
  - On-chip PnP support for audio, joystick port, FM, Modem, MPU-401, CD-ROM, and additional user-defined I/O device.
  - Software address mapping, and DMA and IRQ selections for motherboard implementation.
  - Internal masked PROM support for PnP configuration resource.
- **Dual game ports and timer** – analog timer and digital switches for two joysticks.
- **Hardware volume control interface** – pushbutton inputs for up/down/mute volume control.
- **General-purpose PnP I/O interface** – support for one user-defined PnP device.
- **Modem PnP interface** – control and interface pins for 16-bit enhanced IDE port.
- **IDE CD-ROM interface** – control and interface pins for 16-bit enhanced IDE port.
- **MPU-401 serial port** – asynchronous serial port for MIDI devices such as a wavetable sythesizer or a music keyboard input.
- **Wavetable serial port** – serial port connection from the output of an ES689 or ES690 that eliminates the requirements for an external DAC.
- **DSP serial port** –interface to an optional external DSP for control of the CODEC.
- **ESFM™ FM music synthesizer** – high-quality 20-voice FM synthesizer.

Analog Subsystems

- **Stereo programmable mixer** – six channel stereo mixer.
- **16-Bit stereo game DAC/ADC** – for wavetable and game compatibility.
- **16-Bit stereo music DAC** – for ESFM™ on external wavetable synthesizer.
- **Recording source and input volume control** – input source and volume control for record.
- **Output volume and mute control and record monitor** – analog function control.
- **Reference generator** – analog reference generator.

PNP REGISTERS

Figure 5 shows the configuration register set that is discussed in the following pages. As shown below, the Card-Level registers supported by the ES1868 are the Card-Control Card-Level registers at addresses 00h-07h, and the Vendor-Defined Card-Level registers at addresses 20h-2Fh. The Card-Control Card-Level register at address 07h is a pointer to the Logical Device registers supported by the ES1868 (one set of registers for each logical device on the "card"). In the ES1868, there are six logical devices: the configuration device, the audio+FM+MPU-401 device, the joystick device, the CD-ROM device, the Modem device, and a user-defined General-Purpose device.

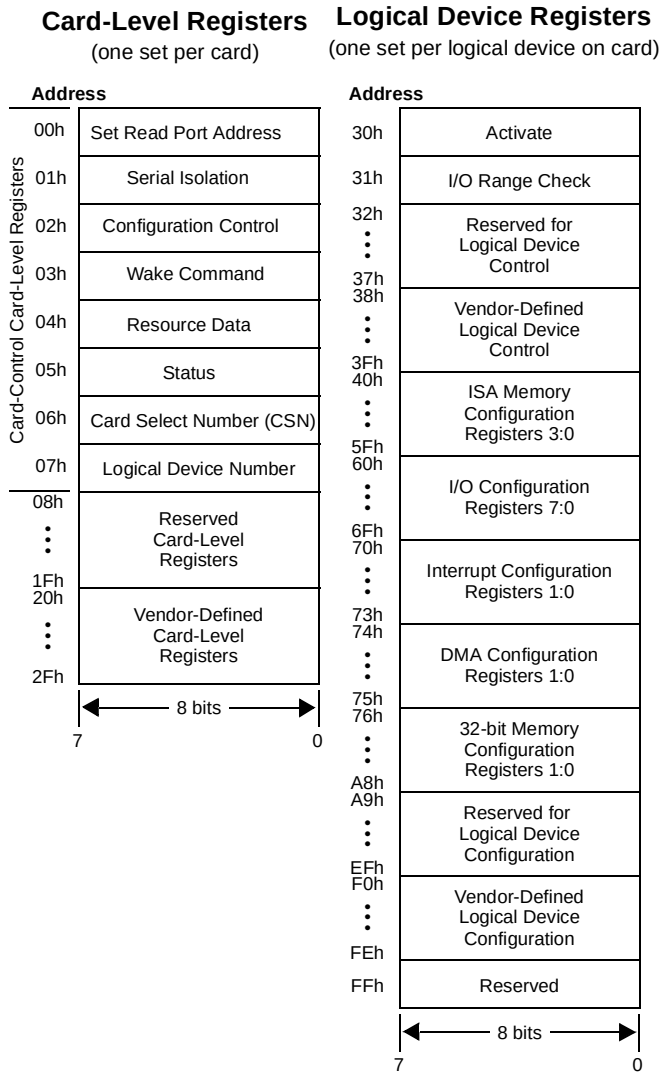


Figure 5 Configuration Register Set

Access to PnP Registers

Configuration Ports

Direct access to PnP registers, effectively bypassing the PnP sequence, can be done by writing a special key sequence to port 279h that depends on bits 6:5 of PnP register 25h, and concluding with two I/O writes to 279h to set the base address of the configuration ports. The key sequence also sets the activate bit for the configuration device.

"Bypass Key"

If PnP is not supported by the system, It is possible to bypass PnP by issuing a special "bypass key" to the ES1868 to force the configuration device to be enabled at a specific I/O address. The ES1868 must be in the "wait-for-key" Plug and Play state. The special key is 32 bytes long, written to the PnP address register (279h). The bypass key must be followed immediately by two I/O writes to the PnP address register to set the low and high bytes of the address register of the configuration device. The configuration device is also activated by the bypass key. The address of the configuration device must be in the range 100h-FF8h and be aligned on a multiple of 8. An "alias" of the audio device address can be used. For example, use E20h for the configuration device if the audio is at 220h.

The actual key sequence is determined by the state of bits 5 and 6 of Vendor-Defined Card-Level register 25h. These bits are both zero after reset, and are loaded from the seventh byte of the PnP ROM header (if the first byte of the header is 'A5'). The purpose of this feature is to handle the case where multiple instances of the ES1868 coexist in a single non-PnP system. It is recommended that all four keys be tried successively. The only difference between the four keys is the two LSBs: XOR bits 1 and 0 of key #0 with bits 5 and 6 of register 25h to generate keys #1, #2, and #3.

Note: The entire sequence should be performed with interrupts disabled in order to minimize the chance that an interrupt will cause the sequence to be corrupted.

Register 25h, bits 6:5 = 0,0

```
66, a1, c2, f1, ea, e7, 71, aa
c7, 63, 33, 1 b, d, 96, db, 6d
a4, 50, 28, 16, 9b, 4d, b6, c9
f4, 78, 3e, 8d, d6, fb, 7f, 3d
<config_address_low>, <config_address_high>
```

Register 25h, bits 6:5 = 0,1

```
67, aO, c3, fO, eb, e6, 70, ab
c6, 62, 32, 1 a, c, 97, da, 6c
a5, 51, 29, 17, 9a, 4c, b7, c8
f5, 79, 3f, 8c, d7, fa, 7e, 3c
<config_address_low>, <config_address_high>
```

Register 25h, bits 6:5 = 1,0

```
64, a3, cO, f3, e8, e5, 73, a8
c5, 61, 31, 19; f, 94, d9, 6f
a6, 52, 2a, 14, 99, 4f, b4, cb
f6, 7a, 3c, 8f, d4, f9, 7d, 3f
<config_address_low>, <config_address_high>
```

Register 25h, bits 6:5 = 1,1

```
65, a2, c1, f2, e9, e4, 72, a9
c4, 60, 30, 18, e, 95, d8, 6e
a7, 53, 2b, 15, 98, 4e, b5, ca
f7, 7b, 3d, 8e, d5, f8, 7c, 3e
<config_address_low>, <config_address_high>
```

Logical Device Numbers

Table 3 Logical Device Numbers

Device	LDN
Configuration device	LDN 0 (mandatory)
Audio device	LDN 1 (mandatory)
Joystick device	LDN 2 (mandatory)
MPU-401	LDN 3 (or LDN 1 I/O descriptor #2) or N.P.
CD-ROM	LDN 3, 4, 5, or N.P.
Modem	LDN 3, 4, 5, or N.P.
General-purpose device	LDN 2, 3, 4, 5, 6, or N.P.

CSN **(06h, Read/Write)**

7	6	5	4	3	2	1	0
card select number							

Read/write card select number. Write only works in isolation mode. Causes transition to Configuration Mode. Read only works in Configuration Mode.

Card-Control Card-Level Registers (08h-1Fh)

Set RD_DATA Port **(00h, Read/Write)**

7	6	5	4	3	2	1	0
Bits 9:2 of the PnP RD_DATA port							

The PnP Read port can be written only when the card is in isolation mode. It is reset low by hardware reset. It can be read only from Configuration Mode.

Serial Isolation **(01h, Read-only)**

7	6	5	4	3	2	1	0
data							

Read-only in isolation state.

Config Control **(02h, Read-only)**

7	6	5	4	3	2	1	0
					RESET_CSN	WFK	SWR

Bit 2 RESET_CSN command.

Bit 1 WAIT_FOR_KEY command.

Bit 0 Software reset command. Does not work in WAIT_FOR_KEY state.

Wake[CSN] **(03h, Write-only)**

7	6	5	4	3	2	1	0
data							

If data written matches CSN, then this card goes from Sleep state to Isolation state if CSN=0 and from Sleep state to Configuration if CSN <> 0.

Resource Data **(04h, Read-only)**

7	6	5	4	3	2	1	0
resource data							

Returns next byte of resource data. Only works in Configuration Mode.

Status **(05h, Read-only)**

7	6	5	4	3	2	1	0
reserved							status

Returns status in bit 0.

Bit 0 0 = not ready.
1 = ready to read resource data. Only works in Configuration mode.

LDN **(07h, Read/Write)**

7	6	5	4	3	2	1	0
logical device number							

Read/write logical device number. Only works in Configuration Mode.

Vendor-Defined Card-Level Registers (20h-2Fh)

IRQB, IRQA **(20h, Read-only)**

7	6	5	4	3	2	1	0
IRQB pin				IRQA pin			

Defines IRQ number assigned to B and A pins. Loaded from Config ROM Header after PnP reset. Unused IRQ pins should be assigned IRQ #1.

IRQD, IRQC **(21h, Read-only)**

7	6	5	4	3	2	1	0
IRQD pin				IRQC pin			

Defines IRQ number assigned to D and C pins.

IRQF, IRQE **(22h, Read-only)**

7	6	5	4	3	2	1	0
IRQF pin				IRQE pin			

Defines IRQ number assigned to F and E pins.

DRQB, DRQA **(23h, Read-only)**

7	6	5	4	3	2	1	0
DRQB pin				DRQA pin			

Defines DRQ number assigned to B and A pins. Loaded from Config ROM header after PnP reset. Unused DRQ pins should be assigned DRQ #2.

DRQD, DRQC **(24h, Read-only)**

7	6	5	4	3	2	1	0
DRQD pin				DRQC pin			

Defines DRQ number assigned to D and C pins.

Configuration ROM Header 0 **(25h, Read-only)**

7	6	5	4	3	2	1	0
DRQ latch	mother-board/card		GP		Modem	CD-ROM	MPU-401

Loaded from Configuration ROM header after PnP reset.

Bit 7 0 = DRQ latch feature disabled.
1 = DRQ latch feature enabled.

Bits 6:5 0 0 = motherboard.
0 1 = card.
1 0 = reserved.
1 1 = reserved.

Bit 4:3 0 0 = GP is not present.
0 1 = GP is LDN 3-6; GP uses 4 addresses.
1 0 = GP uses 8 addresses.
1 1 = GP uses 16 addresses.

Bit 2 0 = Modem not present.
1 = Modem is LDN 3, 4, or 5.

Bit 1 0 = CD-ROM not present.
1 = CD-ROM is LDN 3 or 4.

Bit 0 0 = MPU-401 is part of LDN 1; interrupt is shared with audio int 1 or 2.
1= MPU-401 is LDN 3; interrupt is not shared with audio int 1 or 2.

Configuration ROM Header 1 (26h, Read-only)

7	6	5	4	3	2	1	0
reserved			Ext DMA mask	Audio 2 DMA mask	Audio 1 DMA mask	GPO1	GPO0

Loaded from configuration ROM header after PnP reset.

Bit 4 External DMA mask. 1 = enable.

Bit 3 Audio 2 DMA mask. 1 = enable.

Bit 2 Audio 1 DMA mask. 1 = enable.

Bit 1 0 = GPO1 pin is GPO1.
1 = GPO1 pin is external DACK, GPI is external DRQ.

Bit 0 0 = GPO0 pin is GPO0.
1 = GPO0 pin is GPCS.

Hardware Volume IRQ Number (27h, Read-only)

7	6	5	4	3	2	1	0
Hardware volume IRQ number							

Hardware volume IRQ number (must be shared with audio 1 or audio 2). Reset to 0 by PnP reset.

MPU-401 IRQ Number (28h, Read-only)

7	6	5	4	3	2	1	0
MPU-401 IRQ number							

MPU-401 IRQ number (alias address with register 70h of MPU-401 LDN 3).

Logical Device Registers

LDN0: Configuration Device

Activate Register (30h, Read/Write)

7	6	5	4	3	2	1	0
reserved							Activate

There is one activate register associated with each logical device.

Bit 0 0 = deactivate, 1 = activate.

The default state of this register after reset or after a 1 is written to the reset bit in the card's configuration control bit is 0.

I/O Range Check (31h, Read-only)

7	6	5	4	3	2	1	0
reserved						Enable range check	Pattern select

There is one I/O range check register associated with each logical device. This register verifies that the I/O range assigned to a logical device's I/O address decoders does not conflict with I/O addresses used by another device.

Bit 1 Enable range check: 0 = disable, 1 = enable.

Bit 0 Pattern select: 0 = AAh, 1 = 55h.

I/O Decoder 0 Base Address (60h, Read/Write)

7	6	5	4	3	2	1	0
upper byte							

This register is used to assign an I/O base address to the logical device's I/O decoder 0. I/O base address bits 11:8. If zero, this device is disabled. Eight locations.

I/O Decoder 0 Base Address (61h, Read/Write)

7	6	5	4	3	2	1	0
lower byte							

I/O base address bits 7:0.

DMA 0 (74h, Read-only)

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

DMA 1 (75h, Read-only)

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

LDN1: Audio Device

This device actually supports three functions: audio, FM, and MPU-401. Audio requires sixteen I/O locations, one interrupt which is shared with MPU-401, and two DMA channels. FM requires four I/O locations. MPU-401 requires two I/O locations.

Activate Register (30h, Read/Write)

7	6	5	4	3	2	1	0
reserved							Activate

Bit 0 0 = deactivate (default), 1 = activate.

I/O Range Check (31h, Read-only)

7	6	5	4	3	2	1	0
reserved						Enable range check	Pattern select

This register verifies that the I/O range assigned to a logical device's I/O address decoders does not conflict with I/O addresses used by another device.

Bit 1 Enable range check: 0 = disable, 1 = enable.

Bit 0 Pattern select: 0 = AAh, 1 = 55h.

Audio Processor I/O Base Address (60h, Read/Write)

7	6	5	4	3	2	1	0
upper byte							

I/O base address of audio processor, bits 11:8. If zero, this device is not accessible. Sixteen locations.

Audio Processor I/O Base Address (61h, Read/Write)

7	6	5	4	3	2	1	0
lower byte							

I/O base address of audio processor, bits 7:0.

FM Alias I/O Base Address (62h, Read/Write)

7	6	5	4	3	2	1	0
upper byte							

I/O base address of FM alias, bits 11:8. If zero, this device is not accessible. Four locations.

FM Alias I/O Base Address (63h, Read/Write)

7	6	5	4	3	2	1	0
lower byte							

I/O base address of FM alias, bits 7:0.

MPU-401 I/O Base Address (64h, Read/Write)

7	6	5	4	3	2	1	0
upper byte							

I/O base address of MPU-401, bits 11:8. If zero, this device is not accessible. (MPU-401 may also be accessible through LDN 3). Two locations.

MPU-401 I/O Base Address (65h, Read/Write)

7	6	5	4	3	2	1	0
lower byte							

I/O base address of MPU-401, bits 7:0.

Interrupt Request Level Select 0 (70h, Read/Write)

7	6	5	4	3	2	1	0
data							

Interrupt request level select 0.

(71h, Read-only)

7	6	5	4	3	2	1	0
lower byte							

Returns 2 (low-to-high transition).

Interrupt Request Level Select 1 (72h, Read/Write)

7	6	5	4	3	2	1	0
data							

Interrupt request level select 1.

(73h, Read-only)

7	6	5	4	3	2	1	0
data							

Returns 2 (low-to-high transition).

DMA 0 (74h, Read-only)

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

DMA 1 (75h, Read-only)

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

LDN2: Joystick Device

Activate Register **(30h, Read/Write)**

7	6	5	4	3	2	1	0
reserved							Activate

Bit 0 0 = deactivate (default), 1 = activate.

I/O Range Check **(31h, Read-only)**

7	6	5	4	3	2	1	0
reserved						Enable range check	Pattern select

This register verifies that the I/O range assigned to a logical device's I/O address decoders does not conflict with I/O addresses used by another device.

Bit 1 Enable range check: 0 = disable, 1 = enable.

Bit 0 Pattern select: 0 = AAh, 1 = 55h.

I/O Decoder 0 Base Address **(60h, Read/Write)**

7	6	5	4	3	2	1	0
upper byte							

I/O base address bits 11:8. If zero, this device is disabled. One location.

I/O Decoder 0 Base Address **(61h, Read/Write)**

7	6	5	4	3	2	1	0
lower byte							

I/O base address bits 7:0.

DMA 0 **(74h, Read-only)**

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

DMA 1 **(75h, Read-only)**

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

LDN3: MPU-401 Device

The MPU-401, as an independent device, is optional; normally MPU-401 is part of the *Audio***Drive**®.

Activate Register **(30h, Read/Write)**

7	6	5	4	3	2	1	0
reserved							Activate

Bit 0 0 = deactivate (default), 1 = activate.

The default state of this register after reset or after a 1 is written to the reset bit in the card's configuration control bit is 0.

I/O Range Check **(31h, Read-only)**

7	6	5	4	3	2	1	0
reserved						Enable range check	Pattern select

This register verifies that the I/O range assigned to a logical device's I/O address decoders does not conflict with I/O addresses used by another device.

Bit 1 Enable range check: 0 = disable, 1 = enable.

Bit 0 Pattern select: 0 = AAh, 1 = 55h.

I/O Decoder 0 Base Address **(60h, Read/Write)**

7	6	5	4	3	2	1	0
upper byte							

I/O base address bits 11:8. If zero, this device is disabled. 2 locations.

I/O Decoder 0 Base Address **(61h, Read/Write)**

7	6	5	4	3	2	1	0
lower byte							

I/O base address bits 7:0.

Interrupt Request Level Select 0 **(70h, Read/Write)**

7	6	5	4	3	2	1	0
data							

Interrupt Request Level Select 0.

(71h, Read-only)

7	6	5	4	3	2	1	0
lower byte							

Returns 2 (Low-to-High transition).

DMA 0 **(74h, Read-only)**

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

DMA 1 **(75h, Read-only)**

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

LDN4: CD-ROM Device

The CD-ROM Device is optional. If present, it is LDN 3 or 4.

Activate Register **(30h, Read/Write)**

7	6	5	4	3	2	1	0
reserved							Activate

There is one activate register associated with each logical device.

Bit 0 0 = deactivate (default), 1 = activate.

The default state of this register after reset or after a 1 is written to the reset bit in the card's configuration control bit is 0.

I/O Range Check **(31h, Read-only)**

7	6	5	4	3	2	1	0
reserved						Enable range check	Pattern select

This register verifies that the I/O range assigned to a logical device's I/O address decoders does not conflict with I/O addresses used by another device.

Bit 1 Enable range check: 0 = disable, 1 = enable.

Bit 0 Pattern select: 0 = AAh, 1 = 55h.

I/O Decoder 0 Base Address **(60h, Read/Write)**

7	6	5	4	3	2	1	0
upper byte							

I/O base address of 1st address range, bits 11:8. If zero, this device is not accessible. 8 locations.

I/O Decoder 0 Base Address **(61h, Read/Write)**

7	6	5	4	3	2	1	0
lower byte							

I/O base address of 1st address range, bits 7:0.

CD-ROM I/O Base Address **(62h, Read/Write)**

7	6	5	4	3	2	1	0
upper byte							

I/O base address of FM alias, bits 11:8. If zero, this device is not accessible. Four locations.

CD-ROM I/O Base Address **(63h, Read/Write)**

7	6	5	4	3	2	1	0
lower byte							

I/O base address of FM alias, bits 7:0.

Interrupt Request Level Select 0 **(70h, Read/Write)**

7	6	5	4	3	2	1	0
data							

Interrupt request level select 0.

(71h, Read-only)

7	6	5	4	3	2	1	0
lower byte							

Returns 2 (low-to-high transition).

DMA 0 **(74h, Read-only)**

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

DMA 1 **(75h, Read-only)**

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

LDN5: Modem Device

The Modem Device is optional. If present, it is LDN 3, 4, or 5.

Activate Register **(30h, Read/Write)**

7	6	5	4	3	2	1	0
reserved							Activate

Bit 0 0 = deactivate (default), 1 = activate.

The default state of this register after reset or after a 1 is written to the reset bit in the card's configuration control bit is 0.

I/O Range Check **(31h, Read-only)**

7	6	5	4	3	2	1	0
reserved						Enable range check	Pattern select

This register verifies that the I/O range assigned to a logical device's I/O address decoders does not conflict with I/O addresses used by another device.

Bit 1 Enable range check: 0 = disable, 1 = enable.

Bit 0 Pattern select: 0 = AAh, 1 = 55h.

I/O Decoder 0 Base Address (60h, Read/Write)

7	6	5	4	3	2	1	0
upper byte							

I/O base address of address range, bits 11:8. If zero, this device is not accessible. 8 locations.

I/O Decoder 0 Base Address (61h, Read/Write)

7	6	5	4	3	2	1	0
lower byte							

I/O base address of address range, bits 7:0.

Interrupt Request Level Select 0 (70h, Read/Write)

7	6	5	4	3	2	1	0
data							

Interrupt request level select 0.

(71h, Read-only)

7	6	5	4	3	2	1	0
lower byte							

Returns 2 (low-to-high transition).

DMA 0 (74h, Read-only)

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

DMA 1 (75h, Read-only)

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

LDN6: General-Purpose Device

The general-purpose I/O device is optional. If present, it is LDN 3, 4, 5, or 6.

Activate Register (30h, Read/Write)

7	6	5	4	3	2	1	0
reserved							Activate

Bit 0 0 = deactivate (default), 1 = activate.

The default state of this register after reset or after a 1 is written to the reset bit in the card's configuration control bit is 0.

I/O Range Check (31h, Read-only)

7	6	5	4	3	2	1	0
reserved						Enable range check	Pattern select

This register verifies that the I/O range assigned to a logical device's I/O address decoders does not conflict with I/O addresses used by another device.

Bit 1 Enable range check: 0 = disable, 1 = enable.

Bit 0 Pattern select: 0 = AAh, 1 = 55h.

I/O Decoder 0 Base Address (60h, Read/Write)

7	6	5	4	3	2	1	0
upper byte							

I/O base address of address range, bits 11:8. If zero, this device is not accessible. 4, 8, or 16 locations.

I/O Decoder 0 Base Address (61h, Read/Write)

7	6	5	4	3	2	1	0
lower byte							

I/O base address of address range, bits 7:0.

Interrupt Request Level Select 0 (70h, Read/Write)

7	6	5	4	3	2	1	0
data							

Interrupt request level select 0.

(71h, Read-only)

7	6	5	4	3	2	1	0
data							

Returns 2 (low-to-high transition).

DMA 0 (74h, Read-only)

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

DMA 1 (75h, Read-only)

7	6	5	4	3	2	1	0
data							

Returns 4 (no DMA channel selected).

DMA

The ES1868 incorporates two DMA channels. There are three sources of DMA requests and three targets for DMA acknowledge:

Audio 1 The first audio DMA channel. This DMA channel is used for Sound Blaster-compatible DMA, and extended mode DMA. It can be used for either record or playback. Ideally, this DMA channel should be assigned to ISA channel 1.

Audio 2 The second audio DMA channel. This DMA channel is used for audio playback in full-duplex mode. This channel can be mapped to any of the three 8-bit ISA DMA channels: 0,1, or 3.

External GPO1 can be assigned to be a DMA acknowledge output, GPI can be used as a DMA request input from an external device, either CD-ROM, Modem, or general-purpose device. This channel can be mapped to any of the four DRQ/DACK pairs.

The three DMA sources are mapped to the four DMA pin pairs via Plug and Play (PnP) registers. Also, the four DMA pin pairs are assigned ISA DMA channel numbers via vendor-specific registers 23h and 24h. At least two of the four pin pairs must be assigned to 8-bit ISA DMA channels (0,1, or 3). One or two of the four pin pairs can be assigned to one of the 16-bit ISA DMA channels (5, 6, or 7) for use by the external DMA source.

In order for a DRQ output pin to be *driving* (as opposed to *high-impedance*), two things must occur: 1) The PnP register for the DMA of a given device must match the ISA DMA channel number of the pin and 2) the given device must be activated (that is, bit 0 of PnP register 30h must be high).

External DMA Sharing with Audio DMA

It is possible for an external DMA device to share a DMA channel with the audio if they do not operate at the same time, and the respective Windows drivers can communicate with each other. In this case, the external DMA device does not request a DMA channel in its resource data. The Windows driver writes to the PnP DMA register of the appropriate device to assign it to the same DMA channel as one of the two audio DMA channels.

Bits 4:2 of Vendor-Defined Card-Level register 26h can be used to mask any of the three DMA sources (audio 1, audio 2, and external). Masking can be used when DMA channels are shared to be sure that only one device has access to a given DMA channel at one time.

Full-Duplex (FD) Mode

The ES1868 supports full-duplex DMA in monophonic mode.

In FD mode, the left channel DAC records while the right channel plays back. The ES1868 contains two DMA channels to support this operation.

Programming Full-Duplex Operation

To use FD mode, the first DMA channel is programmed for a mono recording. See the ES1868 DMA programming information for an example. Extended Mode registers A1h and A2h define the sample rate and filter frequency for both record and playback. The record and playback must thus be at the same sample rate (synchronous).

After the first DMA channel is set up, the second DMA channel is programmed. Mixer Extension registers 74h and 76h are set to the 2's complement DMA transfer count. The second DMA channel supports auto-initialize mode as well as normal mode. In auto-initialize mode, which is controlled by Mixer Extension register 78h bit 4, the DMA transfer counter for that channel is automatically re-initialized when it rolls over to zero and the interrupt is reset. In normal mode, initialization must be done under program control.

The playback buffer in system memory does not have to be the same size as the record buffer. When the DMA transfer count rolls over to zero, it can generate an interrupt that is independent of the interrupt generated by the first DMA channel.

If the record and playback buffers are the same size, then a single interrupt can be used. The DMA transfer count registers are programmed with the same value for both channels. The second DMA channel should be enabled before the record channel. For example, assume there are two half-buffers in a circular buffer. When the record channel completes filling the first half, it will generate an interrupt. To ensure that the playback channel is not accessing the first half at the time of the interrupt, start the playback channel first. It has a 32-word FIFO that will be filled quickly via DMA.

The recommended method is:

1. Program both DMA controllers for auto-initialize DMA within separate circular buffers of the same size, N.

- Program the record DMA channel for monophonic, 16-bit recording, auto-initialize mode, but do not set bit 7 of extended register B7h or bit 0 of extended register B8h at this time. Set registers A1h and A2h to define the sample rate and filter frequency, as well as program the 2's complement of the half-buffer size (N/2) into extended registers A4h/A5h.

- Program the playback DMA channel for monophonic, 16-bit playback, auto-initialize mode. Set the 2's complement transfer count for 64 bytes. Since the second channel is in auto-initialize mode, but the second channel interrupt is not being used, any value for the transfer count can be used. Using 64 bytes for the value allows the playback channel to get a “head start” on the record channel by polling the second channel interrupt request bit after starting the second channel DMA.
- Before starting the second channel DMA, clear the second channel interrupt request bit by writing a 0 to bit 7 of Mixer Extension register 7Ah.
- Enable full-duplex mode by setting bit 0 of Mixer Extension register 78h. Since the playback FIFO is presumably empty, the value 0 is transferred to the playback DAC at each sample clock. It is possible that a click or pop will be heard when full-duplex mode is enabled. To prevent this, use the D1h command to enable the DAC input to the mixer after a suitable delay (for example, 25 milliseconds).
- Enable playback DMA by setting bit 1 of Mixer Extension register 78h. After 64 bytes are transferred, bit 7 of 7Ah will go high. Poll this bit with a suitable time-out (for example, 10 milliseconds).
- After bit 7 of 7Ah goes high, enable recording by setting bit 7 of Extended Mode register B7h and bit 0 of Extended Mode register B8h.
- The first 50-100 milliseconds of recorded data should be discarded until analog circuits have settled.

2. To exit full-duplex mode, clear bits 0 and 1 of Mixer Extension register 78h.

The following discusses the registers relevant to full-duplex operation.

DMA-Related Mixer Extension Registers

The following registers control DMA operations:.

Table 4 DMA-Related Programming Registers

Address	Name
74h	Second DMA Transfer Count Reload register – low byte
76h	Second DMA Transfer Count Reload register – high byte
78h	Second DMA control 1
7Ah	Second DMA control 2

DRQ Latch Feature

This feature is enabled when bit 7 of PnP Vendor-Defined Card-Level register 25h is high.

If this feature is enabled, each of the three audio DRQs will be latched high until one of the following occurs:

- A DACK low pulse occurs while DRQ is low or goes low due to a DACK pulse.
- A hardware reset occurs.
- 8-16 milliseconds elapse while DRQ is low.

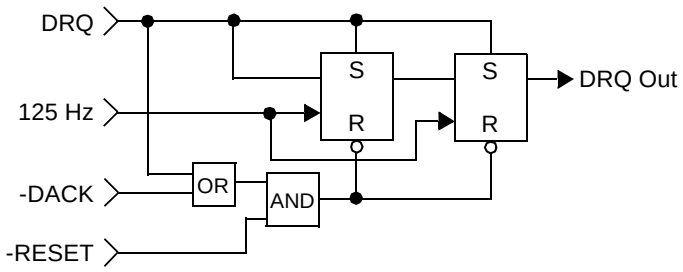


Figure 6 DRQ Latch

INTERRUPTS

There are seven interrupt sources in the ES1868:

Audio 1 Used for the first DMA channel (Sound Blaster-compatible DMA, Extended Mode DMA, and Extended Mode programmed I/O), as well as Sound Blaster-compatible MIDI receive. Extended register B1h controls use of this interrupt for extended mode DMA and programmed I/O. This interrupt request is cleared by hardware or software reset, or an I/O read from port Audio_Base+0Eh. The interrupt request can be polled by reading from port Audio_Base+0Ch. This interrupt is assigned to an interrupt channel by PnP register 70h of LDN 1.

Audio 2 Optional for the second DMA channel. The ES1868 can operate in full-duplex mode using two DMA channels. However, the second DMA channel must share the same sample rate as the first DMA channel. For this reason it is not necessary to use a separate interrupt for the second DMA channel, but it can be done. This interrupt is masked by bit 6 of Mixer Extension register 7Ah. It can be polled and cleared by reading or writing bit 7 of the same register. This interrupt is assigned to an interrupt channel by PnP register 72h of LDN 1.

Hardware Volume
Hardware volume activity interrupt. This interrupt occurs when one of the three hardware volume controls generates an event. Bit 1 of Mixer Extension register 64h is the mask bit for this interrupt. The interrupt request can be polled by reading bit 3 of the same register. The interrupt request is cleared by writing any value to register 66h. This interrupt is assigned to an interrupt channel by PnP register 27h. Typically this interrupt, if used, is shared with an audio interrupt.

MPU-401
This interrupt occurs when a MIDI byte is received. It will go low when a byte is read from the MIDI FIFO and go high again quickly if there are additional bytes in the FIFO. The interrupt status is the same as the read data available status flag in the MPU-401 status register. This interrupt is masked by bit 6 of Mixer Extension register 64h. This interrupt is assigned to an interrupt channel in one of two ways: If the MPU-401 is part of the audio device, then PnP register 28h is used to assign the MPU-401 interrupt. If the MPU-401 is its own logical device, it can also be assigned to an interrupt via PnP register 70h of LDN 3. Both these methods access the same physical register.

CD-ROM This source is the input pin CDIRQ.

Modem This source is the input pin MMIRQ.

General-Purpose
This source is the input pin GPI. If GPI is used for a DMA request for one of the devices CD-ROM, Modem, or General-purpose, then this pin can not be used as a general-purpose device interrupt.

Interrupt sources are mapped to one of the five interrupt output pins through the PnP registers. A given pin can have zero, one, or more interrupts mapped to it. Each PnP pin is assigned to an ISA interrupt channel number by Vendor-Defined Card-Level PnP registers 20h, 21h, and 22h. These registers are automatically loaded from the 8-byte header in the PnP configuration data.

Each interrupt pin can be in either an active or high-impedance state.

If a given interrupt pin has one or more sources assigned to it, and one or more of those sources is activated (register 30h, bit 0), then the interrupt pin will be active, that is, it will always be driving high or low. (An exception is the Modem interrupt, which can be deactivated if input MMIEB is high or if the Modem device is not active.) Each interrupt also has one or more mask bits that are AND'ed with the interrupt request.

Interrupt Status Register

Register 6h of the configuration device can be read to quickly find out which ES1868 interrupt sources are active. The bits are:

Table 5 Interrupt Status Bits in Configuration Register 6

Bit	Description
0	Audio 1 interrupt request
1	Audio 2 interrupt request AND'ed with bit 6 of Mixer Extension register 7Ah
2	Hardware volume interrupt request AND'ed with bit 1 of Mixer Extension register 64h
3	MPU-401 receive interrupt request AND'ed with bit 6 of Mixer register 64h
4	CDIRQ input pin
5	MMIRQ input pin AND'ed with inverse of MMIEB input
6	GPI input pin

Interrupt Mask Register

Register 7h of the configuration device can be used to mask any of the seven interrupt sources.

The mask bits can be used to force the interrupt source to be zero, but they do not put the interrupt pin in a high-impedance state. Each bit is AND'ed with the corresponding interrupt source. This register is set to all ones by hardware reset.

The Interrupt Status Register (ISR) is not affected by the state of the Interrupt Mask Register (IMR). That is, the ISR reflects the status of the interrupt request lines before being masked by the IMR.

The IMR is useful when interrupts are shared. For example, assume that Audio 1, Audio 2, Hardware Volume, and MPU-401 all share the same interrupt in Windows. When returning from Windows to DOS, the Hardware Volume, MPU-401, and Audio 2 interrupts can be masked by setting the appropriate bits to 0.

A second use is within an interrupt handler. The first thing the interrupt handler can do is mask all the interrupt sources mapped to the interrupt handler. Then, the ISR can be polled to decide which sources to process. Just before exiting the interrupt handler, the IMR can be restored. If an unprocessed interrupt remains active, it will generate an interrupt request because the interrupt pin was low during the masked period and then went high when the interrupt sources were unmasked. Also, while the interrupts are masked, the individual interrupt sources can change state any number of times without generating a false interrupt request.

Sharing Interrupts

Plug and Play does not support sharing of interrupts in its resource assignment decision making. If a device wants to share an interrupt with another device that has been assigned an interrupt via PnP, the first device cannot request an interrupt for itself.

A logical device that supports interrupts can be assigned to an interrupt after the PnP sequence by the Windows driver. Refer to the “Bypass Key” section for information on the PnP sequence. In this case, it would typically be forced to share an interrupt with the first audio interrupt. For most cases, this is done simply by programming the appropriate PnP register (70h or 72h) for the selected device. However, there are two special cases.

- The hardware volume interrupt. This interrupt source can be assigned to an interrupt through Vendor-Defined Card-Level register 27h.
- The MPU-401 interrupt. This device is either part of the audio device or its own logical device. If it is part of the audio device, the interrupt can be assigned by writing to Vendor-Defined Card-Level register 28h. If this device is its own logical device, it is assigned an interrupt by either register 28h or register 70h of LDN 3.

PERIPHERAL INTERFACING

DSP/Wavetable Interface

The ES1868 contains a synchronous serial interface for connection to an external DSP or a wavetable music synthesizer.

Applicable Pins

Table 6 identifies pins in the DSP/Wavetable interface.

Table 6 DSP and Wavetable Interface Pins

The following pins are used for interface with an external DSP chip:		
SE	Input with pull-down	Active-high signal from an external DSP to enable serial mode.
DCLK	Input with pull-down	Data clock. The rate can vary, but a typical value is 2.048 MHz (8 kHz x 256).
DX	Tri-state output	Data transmit. Active output when data is being transmitted serially from the ES1868, otherwise high-impedance.
DR	Input with pull-down	Serial data input.
FSX	Input with pull-down	Frame sync transmit. FSX is either active-high or active-low based on bit 3 of Mixer Extension register 48h. The FSX pulse is a request from the external DSP to begin transmission of 8 or 16 bits of data out of pin DX.
FSR	Input with pull-down	Frame sync receive. FSR is either active-high or active-low, based on bit 3 of Mixer Extension register 48h. The FSR pulse signals the arrival of 8 or 16 bits of data to pin DR.
The following pins are used for interface with the ES689/ES690:		
MCLK	Input with pull-down	Serial clock from external ES689/ ES690 music synthesizer (2.75 MHz).
MSD	Input with pull-down	Serial data from external ES689/ ES690 music synthesizer. When both MCLK and MSD are active, the stereo DACs that are normally used by the FM synthesizer are acquired for use by the external ES689/ES690. The normal FM output is blocked.

Applicable Registers

This section lists the Mixer Extension registers related to the DSP and wavetable serial interface operation. These registers are accessed via I/O addresses 2x4h and 2x5h.

Table 7 DSP and Serial Interface Programming Registers

Address	Name
42h	Serial mode input control
44h	Serial mode output control
46h	Serial mode miscellaneous analog control
48h	Serial mode miscellaneous control
4Ch	Serial mode filter divider
4Eh	Serial mode format/source/target

DSP Operating Modes

The DSP interface can be operated in either of two data transfer modes.

Full-Duplex DMA Mode

In this mode, the ES1868's DMA channels are operated in full-duplex (see Figure 7). The DSP port is enabled for mono, 16-bit, receive target = FIFO, and transmit source = FIFO. The sample rate is determined by the externally generated frame sync receive pulses (FSR). In this mode, FSX must equal FSR.

Data transferred via the second DMA channel is written into the second DMA FIFO. From there it is read out one word at a time based on a signal generated from the FSR pulse. The data is transmitted out the DX pin to an external 16-bit CODEC or DSP.

Data received on the DR pin from an external 16-bit CODEC is transferred into the first DMA channel FIFO at a time based on a signal generated from the FSR pulse. From there the data is read out of the first DMA FIFO via first channel DMA cycles.

A typical application of this feature is a software, host-based Modem.

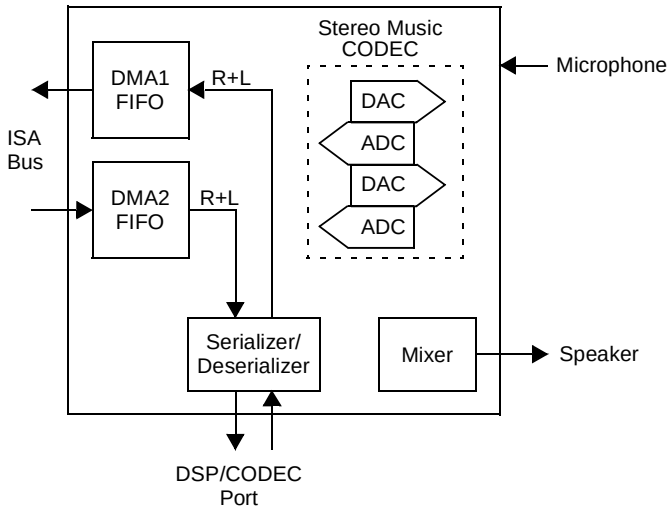


Figure 7 Full-Duplex Mode

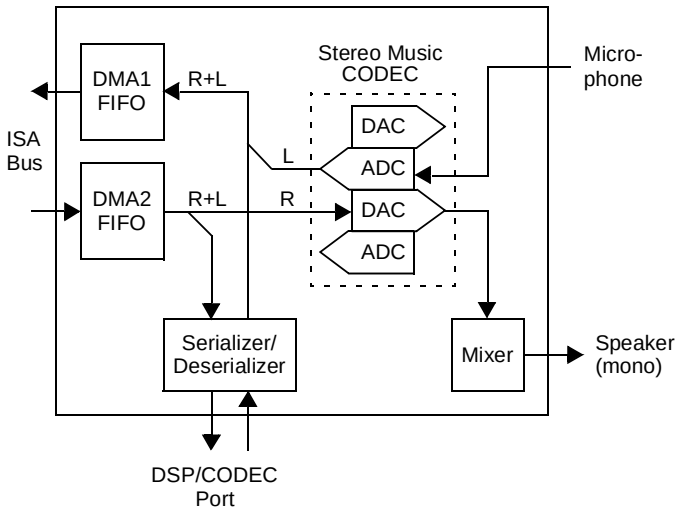


Figure 8 Interleave Mode

Interleave Mode

A typical application of the Interleave Mode is a software, host-based speakerphone, as shown in Figure 8. The host receives data from the phone line, and transmits it to the speaker. It also receives data from the microphone, performs acoustic echo cancellation, and transmits the result to the phone line.

Stereo data is received by the host via the first DMA channel. The “left channel” data comes from the microphone, the “right channel” data comes from the external CODEC.

Stereo data is sent to the ES1868 via the second DMA channel. The “left channel” data is transmitted to the CODEC, the “right channel” data is sent to the speaker.

The Interleave Mode is enabled when both full-duplex DMA is enabled, including the DSP serial interface, and bit 0 of Mixer Extension register 48h is set high.

While the sample rate is determined by the external CODEC, for best results it is recommended to set bit 7 of extended register A1h high. This minimizes jitter between the asynchronous external sync pulses and internal clocks.

Other Modes

A typical Modem application is shown in Figure 9.

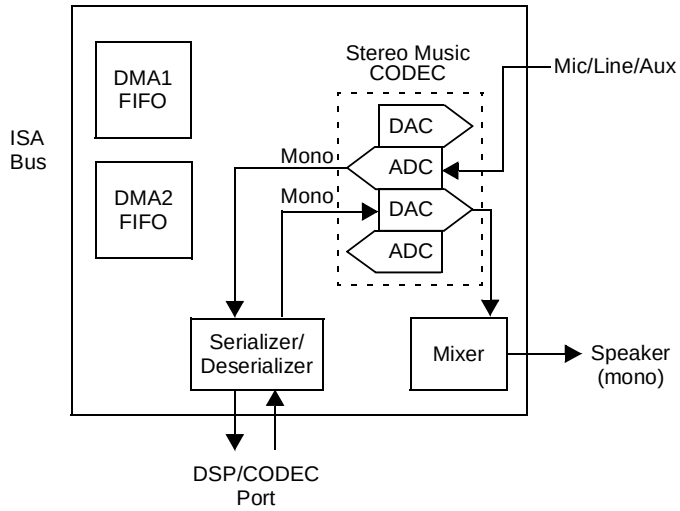


Figure 9 Modem Application

Concurrent Operation of Serial Interface

For the ES689/ES690 interface, the ES1868 detects activity from the ES689/ES690 by the combination of MCLK being active and MSD-toggling within a period of 64 MCLKs. Unless bit 4 of Mixer Extension register 48h is zero, this activity means that the normal FM output is replaced by the signal coming in the serial port. All other ES1868 audio functions are unaffected.

For DSP serial mode (such as enabled by the SE pin), when it is not necessary to use the ES1868 DMA channel as part of the DSP application, then a concurrently running audio application such as a game or a Windows audio application can run without knowledge of the DSP application's acquisition of the analog section. Of course, since the DACs and ADCs are acquired by the DSP, they are not available for the audio application. In this case, sound output from the game or other application will be muted. For example, in a game playing audio data, the DMA from the game will continue to operate normally, but the data will be blocked from the DAC.

Serial Data Format

Figure 10 shows the format for serial data used with the DSP serial interface.

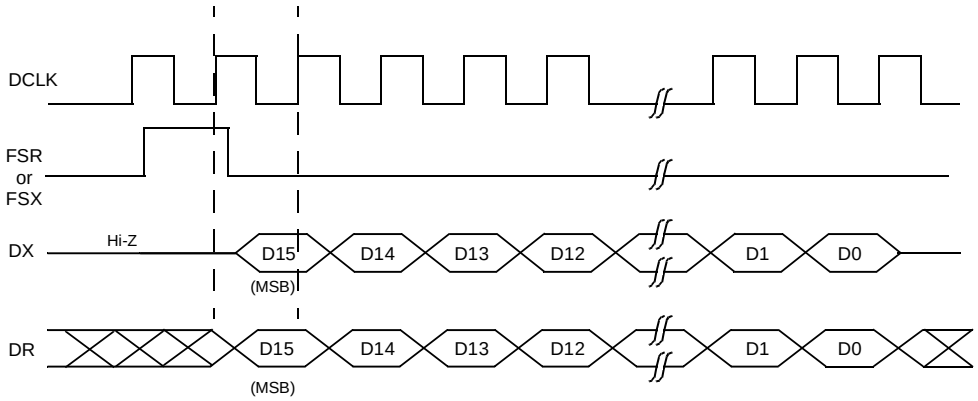


Figure 10 16-Bit Data, Positive Sync Pulse

Modem Interface

The ES1868 supports connection to an external modem.

Applicable Pins

The ES1868 has four pins dedicated to supporting an external modem. They are:

MMCSB Output from the ES1868 to an external modem chip select, active-low. The address space is determined by the PnP configuration. The Modem device uses eight consecutive addresses, with the base address, typically one of the COM ports.

MMIRQ Interrupt request from the Modem device. This signal is mapped to an IRQ output on the ES1868, based on the PnP configuration.

MMIEB Modem interrupt enable input. Active-low when the Modem interrupt is enabled. High when the Modem interrupt request is disabled. Generated from the Modem UART.

GPCS User-defined general-purpose chip select output, If selected by the PnP logic and based on the PnP configuration.

Modem Operating Modes

If the modem DSP also requires a DMA channel, the GPI/GPO1 pins can be used for DRQ/-DACK from the modem.

The modem can also connect to the ES1868 through the DSP serial interface. This allows the modem to set the sample rate for both chips and have access to the microphone and speaker for speakerphone or voice-over-data applications. DSP determines the sample rate of the serial link by generating FSR/FSX pulses.

Figure 11 shows a typical modem interface application, a speakerphone or modem with voice-over-data.

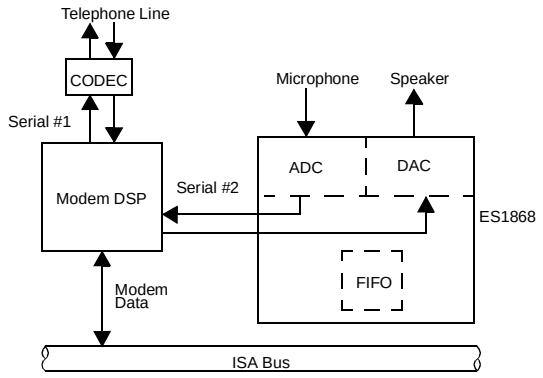


Figure 11 Speakerphone or Modem w/Voice-Over-Data

IDE CD-ROM Interface

Applicable Pins

There are four pins dedicated to supporting an IDE CD-ROM interface.

CDIRQ Interrupt request from CD-ROM. Internally routed to one of the six IRQ ISA outputs (A-F).

CDCSB0 Active-low decode output for eight command block registers. 24 mA driver.

CDCSB1 Active-low decode output for two control block registers. 24 mA driver.

CDENBL Active-low decode output for external 74LS245 transceiver that buffers the least 8 bits of the ISA data bus. This pin is active-low when CDCSB0, CDCSB1, or CD DMA -DACK is active-low.

In most cases, the IDE interface will not use DMA. If it *must* use DMA, then the GPO1/GPI pair (pins 91 and 92) can be used for this purpose. These pins would not be available for other external devices such as a modem/Audio Processor. Also, typically only one of the 4 DRQ/DACK pairs of the ES1868 would be connected to a 16-bit DMA channel. This does not give the PnP system any choice about assigning the CD DMA channel.

It is not recommended to use DMA for the CD-ROM.

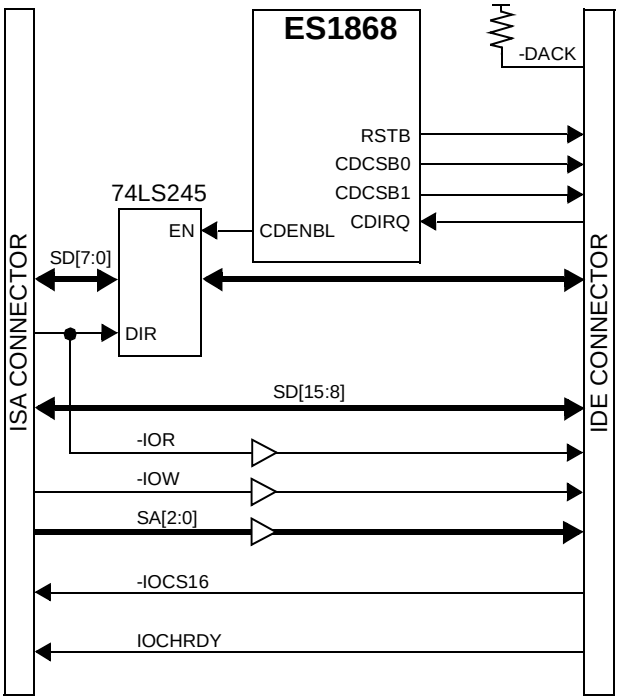


Figure 12 IDE Interface – Typical Application

General-Purpose I/O Device

In addition to modem and CD-ROM interfaces, the ES1868 Plug and Play logic supports one general-purpose I/O device. The GPO0 output can be configured to provide an active-high chip-select output when this device is accessed. The General-purpose device can decode 1, 2, 4, 8, or 16 consecutive addresses.

It is also possible to use GPI/GPO1 as a DMA channel for the General-purpose device if these pins are not used for the Modem or CD-ROM device.

In addition, the GPI pin can be used as an interrupt source for the general-purpose device if the pin is not otherwise used.

Joystick/MPU-401 Interface

Applicable Registers

40H

MPU-401 UART Mode

There are two separate MIDI interfaces in the ES1868. The Sound Blaster compatible command set and a MPU-401 "UART Mode" compatible serial port. MPU-401 is a superior method of MIDI serial I/O because it does not interfere with DAC or ADC Sound Blaster commands. Both methods of serial I/O share the same MSI and MSO pins. The MPU-401 interface consists of separate 8-byte FIFOs for receive and transmit.

By default after hardware reset, the MPU-401 interface is disabled. It must be configured using Mixer Extension register 40h, which is described in the Joystick Device section.

MPU-401 requires an interrupt channel for MIDI receive. This interrupt should be selected using Mixer Extension register 40h. It should be different than the interrupt selected for audio DMA interrupts.

If MPU-401 is enabled, a low-level signal on pin MSI will prevent power-down and cause an automatic wake-up event if the ES1868 is powered down. Likewise, power-down is prevented if a byte is currently being received or transmitted.

Temporarily disabling MPU-401 using Mixer Extension register 40h acts as a reset to the FIFOs.

Joystick/MIDI External Interface

The joystick portion of the ES1868 reference design is identical to that on a standard PC game control adaptor or game port. The PC compatible joystick can be connected to a 15-pin D-sub connector. It supports all standard PC joystick-compatible software. If the system already has a game card or port, either remove the game card or disable the joystick port in the reference design by removing the joystick enable jumper. Disabling the joystick port does not affect its use as a MIDI port.

If support for multiple joysticks is required, a joystick conversion cable is needed. This cable uses a 15-pin D-sub male connector on one end, and two 15-pin D-sub female connector on the other end. All signals on this cable have direct pin-to-pin connection, except for pins 12 and 15. On the male connector, pins 12 and 15 should be left without connection. On the female connectors, pin 15 is internally connected to pin 8, and pin 12 is internally connected to pin 4. The dual joystick port and MIDI port take up only one slot in the system, leaving room for other cards. The dual joystick/MIDI connector configuration is shown below in Figure 13.

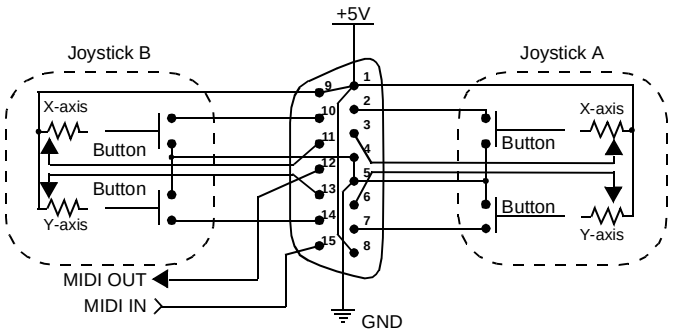


Figure 13 Dual Joystick/MIDI Connector

The MIDI Serial Interface Adaptor from the Joystick/MIDI Connector is shown in Figure 14.

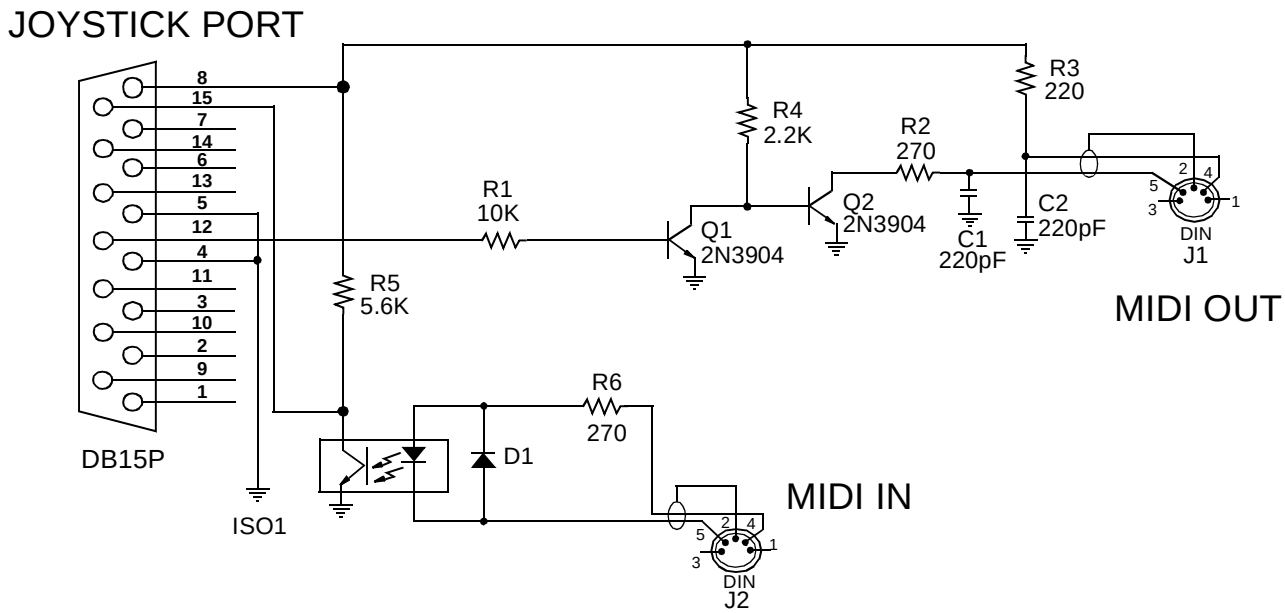


Figure 14 MIDI Serial Interface

Serial EEPROM Interface

The ES1868 gets Plug and Play configuration data from an internal masked ROM or an external EEPROM device. The external EEPROM device is 512K x 8-bit in size.

The EEPROM interface is shared with the hardware volume controls. When the EEPROM interface is active, the volume controls are deactivated. See Figure 15.

The EEPROM can be read or written from the host processor. This allows the EEPROM to be reprogrammed or initially programmed during production test.

Pin 20, when used as SECS, is an input during reset. It is pulled low externally if an EEPROM exists and is to be used. Otherwise, it is pulled high, forcing use of the internal ROM.

After the reset command or hardware reset, 256 bytes from the EEPROM are read into the 256 x 8 FIFO RAM. SECLK becomes an output at 1 MHz. The address sent to the EEPROM will be either 00000000 or 10000000, based on the state of input PSEL.

Depending on the value of pins 25 and 20 and the operating mode selected for these pins, either the internal mask-ROM or the external EEPROM device is used.

PSEL1	SECS/ PSEL0			
0	0	Internal ROM		
1	1	93LC66	512 x 8	9 address bits

EEPROM ROM FORMAT

```
'A5'            Sync Byte
IRQB IRQA       Mapping for IRQB/A
IRQD IRQC       Mapping for IRQD/C
IRQF IRQE       Mapping for IRQF/E
DRQB DRQA       Mapping for DRQB/A
DRQD DRQC       Mapping for DRQD/C
PNP Reg 25h     Miscellaneous
PNP Reg 26h     Miscellaneous
```

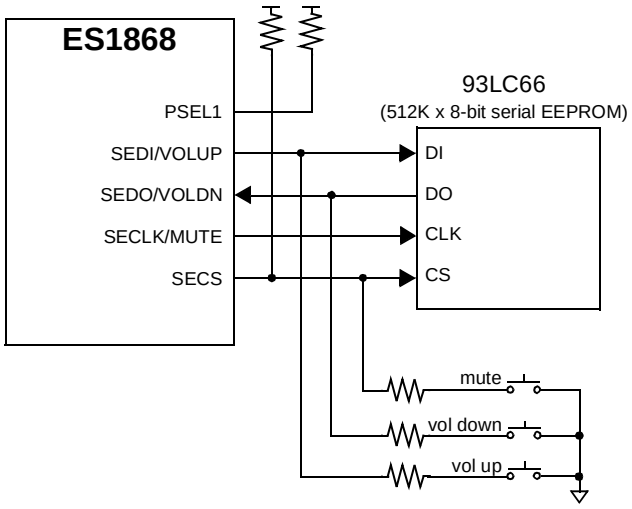


Figure 15 Serial EEPROM – Typical Application

ANALOG DESIGN CONSIDERATIONS

This section describes design considerations related to inputs and outputs of analog signals and related pins on the chip.

Game Port

The game port address 201h is decoded for timer pins TA, TB, TC, and TD, and switch pins SWA, SWB, SWC, and SWD. The MIDI serial input and output also come from the game port connector in most applications.

Reference Generator

Reference generator pins VREF and CMR are shown bypassed to analog ground.

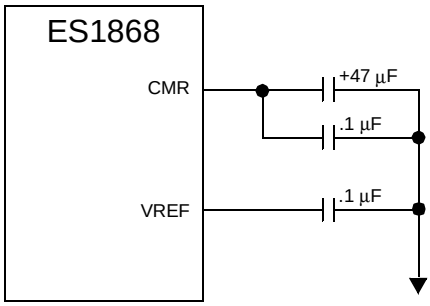


Figure 16 Reference Generator Pin Diagram

Switch-Capacitor Filter

The outputs of the FOUT_L and FOUT_R filters must be AC-coupled to the inputs CIN_L and CIN_R, which provides for DC blocking and an opportunity for low pass filtering with capacitors to analog ground at these inputs.

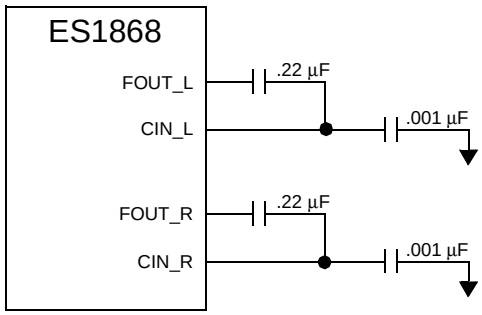


Figure 17 Switch-Capacitor Filter Pin Diagram

Audio Inputs and Outputs

Analog inputs MIC, LINE_L, LINE_R, AUXA_L, and AUXA_R are to be capacitively coupled to their respective input signals. All have pull-up resistors to CMR.

ES1868 analog outputs AOUT_L and AOUT_R are intended to be AC-coupled to an amplifier, volume control potentiometer, or line-level outputs.

POWER MANAGEMENT OPERATING MODES

Overview

The ES1868 supports two normal operating modes and four power-management modes:

- partial power-down mode
- full power-down mode
- self-timed power-down
- suspend/resume state

The decision to power down partially or fully is made by the system processor. To assist the system processor, activity flags are available that can be monitored by the system processor to track I/O activity to and from the ES1868. After a predetermined idle period, the ES1868 can be commanded to power-down partially or fully.

If the oscillator clock is provided from an external circuit, automatic wake-up upon I/O activity is available. With this feature, the act of reading or writing to an ES1868 I/O port will cause the chip to immediately power up without losing context from partial or fully powered-down states.

If the oscillator clock is provided by a crystal, automatic wake-up from partial power-down is still available because the oscillator will continue to run as long as the ES1868 is not fully powered down. Once the chip is fully powered down, however, automatic wake-up is not available with a crystal oscillator due to the start-up requirements of the oscillator itself. It is then the responsibility of the system software to provide for a start-up period for the oscillator before returning control to the application programs that may access the ES1868. In any case, there is no loss of context.

Using GPOs to Indicate Power-Down

The ES1868 has the ability to have one or both of the general-purpose outputs GPO0 and GPO1 change state when the ES1868 is powered-down.

After hardware reset, this feature is disabled and the general-purpose outputs are not affected by power-down. An indirect register in the ES1868 must be programmed to enable this feature.

Specifically, the GPO Power-down Control register is set by command 0CFh to port 227h and read by command 0CEh. It should be set once by system software after system reset. This register will remain unaffected by soft resets. Using this register, one or both of the general-purpose outputs can be programmed to be inverted from their normal state during power-down. The normal state of each pin is set by the appropriate bits in register 227h. A further feature allows the inverted outputs to return to their normal state immediately after power up or after a programmed delay after power-up.

GPO Power-Down Register

7	6	5	4	3	2	1	0
1:restore GPO1 timed	1:invert GPO1 at PDN	1:restore GPO0 timed	1:invert GPO0 at PDN	0	T2	T1	T0

After hardware reset, all bits of this register are 0. This means that GPO0 and GPO1 are unaffected by the power-down status; that is, they remain in the state programmed into register 227h. If bit 6 (GPO1) or bit 4 (GPO0) is high, then the corresponding bit will be inverted from the normal state (register 227h) during power-down.

Bit 7 (GPO1) and bit 5 (GPO0), if low, indicate that the corresponding output will return to its normal state immediately after the ES1868 wakes up from power-down. If high, the corresponding output will return to its normal state after a time period elapses.

The time period is determined by bits 2:0 – T2, T1, T0: A 16 Hz counter will start at 0 and proceed up until it matches the 3-bit number formed by T2, T1, and T0. The maximum delay is 7 * 67 milliseconds or about 469 milliseconds.

Note: "Power-down" as used in this document refers to full power-down, i.e., when both the analog and digital parts of the ES1868 are powered-down.

Partial Power-Down

In the partial power-down mode of operation, the power supply remains connected to the chip during power-down and the chip's analog section remains active while the digital circuits are mostly inactive.

The total current used by the ES1868 can be reduced by a factor of two or more by putting the ES1868 in a partial power-down state. The crystal oscillator, if used, will continue to operate. The analog circuitry remains powered up so that AUXA_L, AUXA_R, AUXB_L, AUXB_R, LINE_L, LINE_R, and MIC audio sources can continue to be heard. FM and DAC audio are automatically muted. There should be no pop when returning from partial power-down to a full power-up state.

The following items are active during partial power-down operation:

1. Oscillator is enabled.
2. MPU-401 operates.
3. PnP operates.
4. Configuration device operates.
5. H/W volume operates.

6. Mixer operates.
7. Analog operates.
8. Joystick operates.
9. Audio device is disabled, FM disabled.
10. Automatic wake-up with any I/O activity to FM or audio registers except 2x4h, 2x5h, 2x6h, 2x7h.

Causing Partial Power-Down

To enter partial power-down mode, bit 3 of register 227h must be high before pulsing bit 2 high, then low, and bit 3 must remain high.

Example: powering down the ES1868 using system software timer interrupt

In this example, it is assumed that the ES1868 is not using a crystal for its clock.

From a timer interrupt routine, read 226h to monitor activity. After one minute of I/O inactivity, it is decided that the ES1868 is to be powered down completely, then return from a timer interrupt. The ES1868 wakes up automatically upon any I/O access to the ES1868 by any application.

1. First, see if the ES1868 is already powered down (bit 3 of port 226h = 0). If so, there is nothing to do.
2. Next, check if the ES1868 is being held in reset by reading bit 0 of port 226h. If bit 0 is high, the reset must be released before power-down can occur: Clear bit 0 of port 226h, then delay 1 millisecond or more for the ES1868 processor to complete its initialization.
3. Next, check to see if the ES1868 is in MIDI serial interface mode by testing bit 2 of port address 226h. If so, it may not be prudent to power-down. While the ES1868 can power-down when in MIDI mode, it will not automatically wake up if serial data comes in to the MSI pin, and such data will be lost.
4. Next, send a power-down request to the chip by clearing bit 3 in register 227h, then pulsing bit 2 first high, then low. The other bits of this register should be preserved. The ES1868 processor sees the rising edge of bit 2 of register 227h as an interrupt request to power-down.

Waking from Partial Power-down

Any I/O activity will wake the ES1868 from a partial power-down. The following items are in effect upon waking from partial power-down:

- CSAUD + I/O except 2x6h read, 2x7h read/write.
- CSFM + I/O.
- Audio DACK + I/O.
- DSP or ES689/ES690 Serial Activity.

Full Power-Down

Complete power-down reduces the operating current to less than 50 microamps.

The following items are indicators of a full power-down operation:

- Nothing operates, except for some programmed I/O.
- The Activity Flags from a port 2x6h read are:

  Bit 7 Activity latch PnP, Joystick, MPU-401, Configuration, CD-ROM, Modem, or GPI/O or DMA activity.

  Bit 6 Activity latch: 2x4h, 2x5h I/O.

  Bit 5 Activity latch: Audio (except 2x4h, 2x5h, 2x6h read, 2x7h read/write), FM I/O or DMA.

  Bit 4 DSP and ES689/ES690 serial activity status.

Wake from Total Power-Down

There are three main ways to wake the chip up from full power-down:

1. hardware reset
2. software reset
3. I/O activity

Hardware Reset

The chip is automatically restored to activity upon a hardware reset. Context is not preserved.

Software Reset

Refer to the section “Resetting the ES1868 via Software” for information on the software reset sequence.

I/O Activity Causing Automatic Wake-up

Automatic wake-up is the method whereby the chip returns to the full power-up state, triggered by I/O activity. With automatic wake-up the context is preserved.

Any I/O access to any of the ES1868 port addresses other than 226h or 227h causes an automatic wake-up.

Automatic wake-up can also be triggered by DMA accesses. However, it is unlikely this will occur if power-down is triggered by a period of I/O inactivity, which includes DMA accesses and the I/O operations required to set up the DMA transfer.

Automatic wake-up requires that XI or EXTCLK is driven by a stable clock. This can either be an external clock source or from a crystal connected to XI and XO. In the latter case, the ES1868 cannot be fully powered down and have automatic wake-up work correctly. This is because the oscillator will require some time (typically greater than 25 milliseconds) to stabilize.

In the full power-down state the oscillator is stopped and the analog circuitry is powered down. The AOUT_L and AOUT_R pins are left at approximately the reference voltage by a high value resistor divider.

To wake the chip from a total power-down, set bit 4 of port 227h high for 25 milliseconds, then clear bit 3, ENXOSC, of port 227h. This enables the oscillator even when analog is powered down.

Inputs and Outputs During Power-Down

When powered-down, digital inputs that do not have pull-up or pull-down devices should be pulled high or low, that is, they should not be floating. An example would be placing pull-down resistors on pins such as A[11:0] and AEN.

Some input pins have circuitry that provides a pull-down device when the ES1868 digital circuits are powered up. During power-down, these inputs have a feedback device that latches the input state and prevents leakage current into the pin, effectively disabling the pull-down device. The pins that have this feature are SE and DR.

The CE pin has a similar feature using a pull-up device rather than a pull-down device.

Output pins such as DRQx and IRQx will be frozen in their state at power-down.

GPO0 and GPO1 may change state during full power-down if so programmed (see section below on programming GPO0 and GPO1 to reflect power-down status).

The MSI pin has an internal pull-up device, so this pin can be left floating during power-down.

The internal inverter connected to pins XI and XO will continue to operate when the digital portion of the ES1868 is powered-down as long as 1) SCLK is high, and 2) the analog portion is powered-up. When the chip is fully powered-down, the inverter becomes high-impedance with a weak pull-up on the XO pin.

The VREF output is driven low when the analog circuitry is powered-down.

CMR is pulled low by an internal transistor during analog power-down.

The AOUT_L and AOUT_R pins will be held at approximately the idle voltage level with a high-impedance resistor divider. After return to full power-up state from full power-down state, these pins are not enabled for 48-64 milliseonds. The chip should remain in full power-up state for at least 64 milliseconds to assure that the AOUT_L and AOUT_R pins are enabled before changing to the partial power-down state. Otherwise they may never get enabled. For this reason it is not possible to go directly from full power-down to partial power-down and have AOUT_L and AOUT_R enabled.

Self-Timed Power-Down

The ES1868 processor can be programmed to monitor I/O activity in place of the system processor, and after a programmable period of inactivity, enter either a partial or full power-down state. Whether the ES1868 enters a partial or full power-down is determined by bit 3 of port 227h.

In this case, power is maintained as for partial or full power-down, except the decision to power-down is made by the ES1868 itself. In self-timed power-down, the ES1868 processor waits for a pre-programmed period of I/O inactivity between successive commands before entering partial or full power-down state. This mode is otherwise similar to partial or full power-down except that the decision to power-down is made by the ES1868 processor rather than the system processor. Even if self-timed power-down is enabled, the ES1868 can becommanded to power down by bit 2 of port 227h.

The ES1868 requires use of the activity flags in register 226h. Therefore, if this feature is enabled, the system processor will not be able to monitor I/O activity.

Enabling Self-Timed Power-Down

1. Send command C6h to enable access to this feature using the BDh command.
2. Send command BDh.
3. Send the time out value N, where the time period is N x 8 seconds. If the value N is zero, self-timed power-down is disabled.
4. Send command C7h to disable access to this feature by the BDh command.

There is one limitation to this feature: the timing of inactivity only occurs between commands sent to the ES1868. It is possible for a program to leave the ES1868 in a state where timing will not happen. An example of this is if a program exits without completion of a DMA transfer. Most programs are well-behaved in this respect and leave the ES1868 with appropriate registers defined.

Suspend/Resume

In the fourth power management category, power is removed from the ES1868 during its suspended state. Before removing power, the entire context of the processor and registers must be uploaded to the system processor and saved. After restoring power and generating a hardware reset, the opposite resume operation must download the context.

The term “suspend” is used here to describe the process of uploading the context of the ES1868 and removing digital

and analog power to the chip. The term “resume” describes the process of applying power to the ES1868 and downloading the context.

In firmware version 10 of the ES1868, 782 (decimal) bytes are required to store the entire context of the ES1868.

It is possible to suspend the ES1868 regardless of its current state, including suspending in the middle of a DMA transfer. The suspend process is initiated by pulsing bit 7 of port address 227h high, then low. This will interrupt the ES1868 processor and begin a sequence of upload operations.

A hardware reset is required during the resume procedure, before downloading the context. Downloading the context is initiated with command C1h.

A sample assembly language program that implements suspend and resume from a TSR is available from the applications department of ESS Technology.

Pop Prevention in the External Amplifier

Normally, in order to directly drive speakers in an ES1868 design, an external stereo amplifier chip is used. There are two power management problems associated with an external amplifier:

1. The amplifier itself will draw current unless it can be powered down.
2. Suspend/resume will cause pops because power is removed from the ES1868 and then re-applied.

Amplifiers such as the SGS/Thomson TDA7233 have a mute input which reduces current to 400 microamps and also reduces pops from the suspend/resume process. This part is a mono amplifier, so two are required. Connect GPO0 to the active low MUTE input of the TDA7233. In this case the amplifier will be muted after hardware reset. In an program activated from the AUTOEXEC.BAT file, program the ES1868 so that GPO0 will be high when powered-up and low when fully powered-down. Program a delay of about 133 milliseconds between power-down and power-up states, before GPO0 returns high, to allow the ES1868 analog circuits to stabilize.

Power Management and the FM Synthesizer

The ES1868 FM synthesizer is a fully static design. This means that the clock can be stopped to power-down the circuitry without loss of the state.

Also, for suspend/resume applications, the entire context of the synthesizer can be read back. The details of this procedure are beyond the scope of this document and are covered in an application note concerning suspend/ resume.

NORMAL OPERATING MODES

The ES1868 can be in one of two operating modes: (Sound Blaster) Compatibility Mode, and (ESS) Extended Mode.

In both modes, a set of mixer control registers allows application software to control the analog mixer, record source, and output volume. Programming the ES1868 Enhanced Mixer is described later in this document in the section on programming in Extended Mode.

Compatibility Mode Description

As shown in Table 8, there are two ways to access the ADCs and DACs inside the ES1868. The first mode is called Compatibility Mode, where the ES1868 is compatible with both the ES488 and the Sound Blaster Pro. This is the default mode after any reset. In this mode the ES1868 processor is an intermediary in all functions between the ISA bus and the ADC and DAC. The blocks labeled “FIFO/DMA Control” and “256-Byte FIFO” are inactive. The ES1868 processor performs limited FIFO functions using 64 bytes of internal memory.

Extended Mode Description

The ES1868 also supports an Extended Mode of operation. In this case a 256-byte FIFO is used as an intermediary between the ISA bus and the ADC and DAC control registers, and various Extended Mode indirect registers are used for control. The ES1868 processor is mostly idle in this mode. DMA control is handled by dedicated logic. Programming for Extended Mode operation requires accessing various control registers with ES1868 commands. Some of these commands are also useful for Compatibility Mode, such as those that configure DMA and IRQ channels. Table 8 lists the features of the two modes.

Table 8 Comparison of Operation Modes

	Compatibility Mode (Sound Blaster Pro)	**Extended Mode**
Sound Blaster Pro compatible	Yes	No
FIFO Size	64 bytes (firmware managed)	256 bytes (hardware managed)
Mono 8-bit ADC, DAC	Yes, to 44 kHz	Yes, to 44 kHz
Mono 16-bit ADC, DAC	Yes, to 22 kHz	Yes, to 44 kHz
Stereo 8-bit DAC	Yes, to 22 kHz	Yes, to 44 kHz
Stereo 8-bit ADC	Yes, to 22 kHz	Yes, to 44 kHz
Stereo 16-bit DAC	Yes, to 11 kHz	Yes, to 44 kHz
Stereo 16-bit ADC	No	Yes, to 44 kHz
Signed/Unsigned Control	No	Yes
Automatic Gain Control during recording	Firmware controlled, to 22 kHz, mono only	No
Programmed I/O block transfer for ADC and DAC	No	Yes
FIFO status flags	No	Yes
Auto reload DMA	Yes	Yes
Time base for programmable timer	1 MHz or 1.5 MHz	800 kHz or 400 kHz
ADC and DAC jitter	± 2 microseconds	None

PROGRAMMING THE ES1868

Identifying the ES1868

The ES1868 may be identified by reading Mixer Extension register 40h successively. It returns the following values on four successive reads:

18h, 68h, A[11:0], A[7:0]

where 18h and 68h are data reads indicating the part number (1868), and A[11:0] is the base address of the configuration device.

Resetting the ES1868 via Software

The chip can be reset in either of two ways: hardware reset and software reset. The hardware reset signal comes from the ISA bus. Software reset is controlled by bit 0 of port 2x6h.

To reset the ES1868 by software:

1. Write a 1 to port 2x6h.
2. Delay a short period, for example, by reading back 2x6h.
3. Write a 0 to port 2x6h.
4. In a loop that lasts at least 1 milliseconds, poll port 2xEh bit 7 for read data availability.

   If bit 7 is high, read the byte from port 2xAh. Exit loop if the content is 0AAh; otherwise, continue polling.

Both hardware reset and software reset will:

1. Disable Extended Mode.
2. Reset the timer divider and filter registers for 8 kHz sampling.
3. Stop any DMA transaction in progress.
4. Clear any active interrupt request.
5. Disable voice input of mixer (see the D1h/ D3h commands).
6. Reset Compatibility Mode and Extended Mode DMA counters to 2048 bytes.
7. Set analog direction to be DAC, with the DAC value set to mid-level.
8. Set input volume for 8-bit recording with Automatic Gain Control (AGC) to maximum.
9. Set input volume for 16-bit recording to mid-range

In addition to performing actions on the above list, a hardware reset will reset all Mixer registers to default values.

Configuring the ES1868

PnP Configuration

The ES1868 can be configured using the Configuration registers, which are Direct registers. These registers are listed in Table 9.

Table 9 Configuration Registers

Address Offset	Name	Bits	Function	Values
Base+0h	Configuration register address			
Base+1h	Configuration register data			
Base+2h	EEPROM data register			
Base+3h	EEPROM command register	Bits 3:0	Command	0 0 0 0 = Write disable 0 0 0 1 = Write all 0 0 1 0 = Erase all 0 0 1 1 = Write enable 0 1 0 0 = Write 1 0 0 0 = Read 1 1 0 0 = Erase
Base+4h	Reset EEPROM address			
Base+5h	Status register	Bit 0 Bit 1 Bits 3:2 Bits 5:4	Reset sequence busy bit PNPOK bit State EEPROM type	 00 = wait_for_key 01 = sleep 10 = isolation 11 = configure 00 = internal ROM 11 = 512 x 8-bit
Base+6h	Interrupt Status register	Bit 0 Bit 1 Bit 2 Bit 3 Bit 4 Bit 5 Bit 6 Bit 7	Audio 1 Audio 2 Hardware volume MPU-401 CD-ROM interface Modem General-purpose reserved	
Base+7h	Interrupt Mask register	Bit 0 Bit 1 Bit 2 Bit 3 Bit 4 Bit 5 Bit 6 Bit 7	Audio 1 Audio 2 Hardware volume MPU-401 CD-ROM Interface Modem General-purpose reserved	

Compatibility Mode Programming

This section describes Compatibility Mode programming considerations.

Compatibility Mode DAC Operation

After reset, the analog circuitry is set up for DAC operations. Any ADC command will cause a switch to the ADC "direction," and any subsequent DAC command will switch the ES1868 back to the DAC "direction." The DAC output is filtered and connected to the voice input of the mixer. After reset, the voice input to the mixer is muted to prevent pops. The ES1868 maintains a status flag called the Voice-Enable/Disable flag that indicates when the voice channel is muted. Use command D1h to enable the voice channel and command D3h to disable the voice channel.

If you do not wish to reset the ES1868 before playing a new sound, and you are not certain of the status of the analog circuits, you can mute the voice input to the mixer with command D3h, then set up DAC direction and level using the direct-to-DAC command:

10h + 80h

Then wait 25 milliseconds for the analog circuitry to settle before enabling the voice channel with command D1H.

A pop sound may still be heard if the DAC level was left at a value other than mid-level (code 80h on an 8-bit scale) by the previous play operation. To prevent this, always finish a DAC transfer with a command to set the DAC level to mid-range:

10h + 80h

8-Bit, 16-Bit, and Compressed Data Formats

The 8-bit samples are unsigned, ranging from 0 to 0FFh, with the DC level around 80h.

16-bit samples are unsigned, least byte first, ranging from 0000h to 0FFFFh with the DC level around 8000h.

The ES1868 supports two types of compressed sound DAC operations: **ESPCM**®, which uses a variety of proprietary compression techniques developed by ESS Technology, and ADPCM, which is supported by many other sound cards but is of a lower quality.

Both ADPCM and **ESPCM**® are only transferred using DMA transfer. The first block of a multiple-block transfer uses a different command than subsequent blocks. The first byte of the first block is called the reference byte.

Direct Mode DAC vs. DMA Mode DAC

In direct mode, the timing for DAC transfers is handled by the application program. For example, the system timer can be reprogrammed to generate interrupts at the desired sample rate. At each system timer interrupt, the command 10h (or 11h for 16-bit data) is issued followed by the sample. Polling of the Write-Buffer-Available flag is required before writing the command and between the command and the data.

Note: The switched capacitor filter is initialized by reset for an intended sample rate of 8 kHz. In direct mode, the application may wish to adjust this filter appropriate to the actual sample rate. The easiest way to do this is to program the timer with command 40h just as if the application were using DMA mode.

In DMA mode, the programmable timer in the ES1868 controls the rate at which samples are sent to the DAC. The timer is programmed using command 40h, which also sets up the programmable filters inside the ES1868. The ES1868 firmware maintains an internal FIFO (32 levels for 16-bit transfers, 64 levels for 8-bit transfers) that is filled by DMA transfers and emptied by the timed transfers to the DAC.

Before a DMA transfer, the application first programs the DMA controller for the desired transfer size and address, then programs the ES1868 with the same size information. At the end of the transfer, the ES1868 generates an interrupt request, indicating that the current block transfer is complete. The FIFO gives the application program sufficient time to respond to the interrupt and initiate the next block transfer.

In "normal mode" DMA transfers, the DMA controller must be initialized and the ES1868 be commanded for every block that is transferred. In "auto-initialize mode", the DMA transfer is continuous, in a circular buffer, and the ES1868 generates an interrupt for the transition between buffer halves. In this mode the DMA controller and ES1868 need to be set up only once.

The ES1868 supports mono 8-bit transfers to DAC at a rate up to 44 kHz. Mono 16-bit transfers are supported up to a rate of 22 kHz.

Stereo DAC Transfers in Compatibility Mode

Stereo DAC transfers are only available using DMA rather than direct mode commands.

To perform a stereo DAC transfer, first set bit 1 of Mixer register 0Eh high. Then set the timer divider to twice the per-channel sample rate. The maximum stereo transfer rate for 8-bit data is 22 kHz per channel, so for this case program the timer divider as if it were for 44 kHz mono. The maximum stereo transfer rate for 16-bit data is 11 kHz per channel.

For 8-bit data, the ES1868 expects the first byte transferred to be for the right channel, and subsequent bytes to alternate left, right etc.

For 16-bit data, the ES1868 expects the DMA transfers to be a multiple of 4, with repeating groups in the order:

1. left low byte
2. left high byte
3. right low byte
4. right high byte

Clear bit 1 of Mixer register 0Eh when the DAC transfer is complete.

Compatibility Mode ADC Operation

The ES1868 analog circuitry is switched from the DAC direction to the ADC direction by the first direct or DMA mode ADC command. Discard the first 25 to 100 milliseconds of samples if possible because pops might occur in the data due to the change from the DAC to ADC direction. In the ADC direction the voice input to the mixer is automatically muted.

The ES1868 has four recording sources: Microphone, Line, Aux/CD, and Mixer. Microphone input is the source after any reset. Select the source using the mixer control register 0Ch/1Ch.

The selected source passes through an input volume stage that can be programmed with 16 levels of gain from 0 to +22.5 dB in steps of 1.5 dB. In 8-bit recordings (other than “high speed mode”) the volume stage is controlled by the ES1868 firmware for the purposes of AGC. In 16-bit recordings as well as “high speed mode” 8-bit recordings, the input volume stage is controllable from application software. Use command DDh to set the input volume level from 0 to 15. The reset default is mid-range, 8.

The ES1868 supports direct mode ADC, “normal mode” DMA for ADC, as well all “auto-initialize mode” DMA for ADC. The differences between the various types are described above for DAC.

Note: The switched capacitor filter is initialized by reset for an intended sample rate of 8 kHz. In direct mode, the application may wish to adjust this filter appropriate to the actual sample rate. The best way to do this is to program the timer with command 40h just as if the application was using DMA mode.

The maximum sample rate for direct mode ADC is 22 kHz.

The maximum sample rate for DMA ADC for both 8-bit and 16-bit is 22 kHz, using commands 24h, 25h, 2Ch or 2Dh.

There is a special “high speed mode” for ADC that allows 8-bit sampling up to 44 kHz. This mode uses commands 98h (auto-initialize) and 99h (normal). No AGC is performed: the input volume is controlled with command DDh.

Sending Commands During Compatibility Mode DMA Operations

The ES1868 has an internal 64-byte FIFO used for DMA to the DAC and from the ADC. When the FIFO is full (in the case of DAC, empty in the case of ADC), DMA requests are temporarily suspended and the Busy flag (bit 7 of port 2xCh) is cleared. This allows a window of opportunity to send a command to the ES1868. Commands such as D1h and D3h control the mixer Voice-Enable/Disable status, and command D0h suspends or pauses DMA.

The ES1868 chip sets the Busy flag when the command window is no longer open. Application software must send a command within 13 microseconds after the Busy flag goes high or the command will be confused with DMA data. This is normally easy to do if the polling is done with interrupts disabled.

As an example of sending a command during DMA, consider the case where the application desires to send command D0h in the middle of a DMA transfer. The application disables interrupts and polls the Busy flag. Because of the FIFO and the rules used for determining the command window, it is possible for the current DMA transfer to complete while waiting for the Busy flag to clear. In this event, the D0h command has no function, and a pending interrupt request from the DMA completion is generated. The interrupt request can be cleared by reading port 2xEh before enabling interrupts.

Figure 18 shows timing considerations for sending a command.

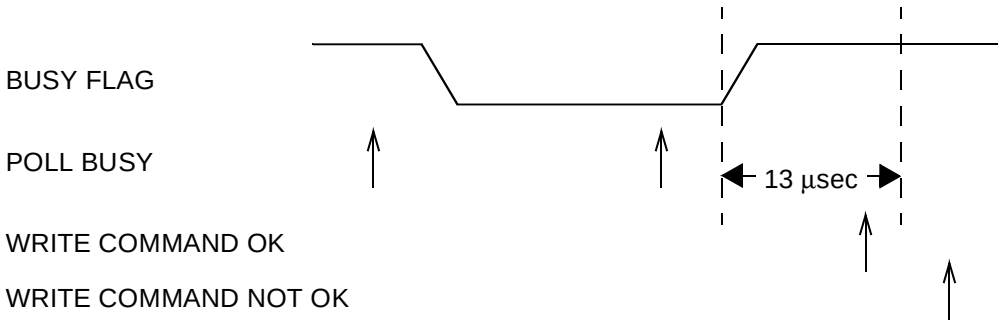


Figure 18 Command Transfer Timing

Extended Mode Programming

This section describes Extended Mode programming considerations.

Extended Mode registers are indirect registers, that is, they are written to and read from using commands sent to a port.

Mixing Modes Not Recommended

Avoid mixing Extended Mode commands with Compatibility Mode commands where possible. The Voice-Enable/Disable commands D1h and D3h are safe to use when using Extended Mode to process ADC or DAC. However, there are other Compatibility Mode commands that are likely to cause problems. The Extended Mode commands may be used to set up just the DMA or IRQ channels before entering the Compatibility Mode.

Commanding the ES1868 Extended Registers

This section describes how to send commands and command-related data to the ES1868's extended registers, which are indirect registers.

Enabling Extended Mode Commands

After any reset, and before using any Extended Mode commands you must first send command C6h to enable Extended Mode operation.

Commands of the format Axh or Bxh, where x is a numeric value, are used for Extended Mode programming, and are used to access the 'internal' or *indirect* registers of the ES1868. For convenience, the registers are named after the commands used to access them. For example, "register A4h", the DMA counter low byte register, is written to via "command A4h".

Writing ES1868 Internal Registers

The following show an example of writing to an ES1868 internal: to set up the FIFO DMA Counter Reload register to F800h, send the following command/data bytes:

A4h, 00h; register A4h = 0h
A5h, F8h; register A5h=F8h

Always check the write buffer before writing a command to port 2xCh, to make sure it is not busy. Also, be sure to send command C6h after every reset when using Extended Mode commands.

Reading ES1868 Internal Registers

Command C0h is used to read the ES1868 internal registers in Extended Mode. Send command C0h followed by the register number, Axh or Bxh. For example, to read register A4h, send the following command bytes:

C0h, A4h

Then poll the Read-Data-Buffer-Status bit, bit 7 of port 2xEh, before reading the register contents.

Command/Data Handshaking Protocol

Writing Commands to the ES1868

Commands written to the ES1868 enter a write buffer. Before writing the command, make sure the buffer is not busy.

Bit 7 of port 2xCH is the ES1868 Busy flag. It is set when the write buffer is full or when the ES1868 is otherwise busy (for example, during initialization after reset or during Compatibility Mode DMA requests).

To write a command or data byte to the ES1868 processor:

1. poll bit 7 of port 2xCh until it is clear
2. write the command/data byte to port 2xCh.

Note: The port 2xCh Write Buffer is shared with Compatibility Mode DMA write operations. When DMA is active, the Busy flag is cleared during time windows when a command can be received. Normally, the only commands that should be sent during DMA operations are 0Dxh commands such as DMA-Pause/Continue, Voice-Enable/Disable, etc. In this situation it is recommended that interrupts be disabled between the time that the Busy bit is polled and the command is written. Also, the time between these instructions should be minimized. For more information, see the section titled "Sending Commands During Compatibility Mode DMA Operations".

Reading the Read Data Buffer of the ES1868

The Read-Data-Buffer-Status flag can be polled by reading bit 7 of port 2xEh. When a byte is available the bit is set high. Note that any read of port 2xEh will also clear any active interrupt request from the ES1868. An alternative way of polling the read buffer status bit is via bit 6 of port 2xCh, which is the same flag. The buffer status flag is cleared automatically by reading the byte from port 2xAh.

Summary of Commands for Extended Mode

When the ES1868 is in Extended Mode, it accepts commands for the extended (indirect) registers.

Table 10 lists the commands accepted by the ES1868 in this mode.

Table 10 Command Summary

Command	Data Byte(s) Write/Read	Function
10h	1 write	Direct write 8-bit DAC. Data is 8-bit unsigned format.
11h	2 writes	Direct write 16-bit DAC. Data is 16-bit unsigned format, first low byte then high byte.
14h	2 writes	Start normal mode DMA for 8-bit DAC transfer. Data is transfer count - 1, least byte first. Stereo DAC transfer if stereo flag is set in Mixer register 0Eh. Maximum sample rate is 44 kHz mono, 22 kHz stereo.
15h	2 writes	Start normal mode DMA for 16-bit DAC transfer. Data is transfer count - 1, least byte first. Stereo DAC transfer if stereo flag is set in Mixer register 0EH. Maximum sample rate is 22 kHz mono, 11 kHz stereo.
1Ch		Start auto-initialize mode DMA for 8-bit DAC transfer. Block size must be previously set by command 48h. Stereo DAC transfer if stereo flag is set in Mixer register 0Eh. Maximum sample rate is 44 kHz mono, 22 kHz stereo.
1Dh		Start auto-initialize mode DMA for 16-bit DAC transfer. Block size must be previously set by command 48h. Stereo DAC transfer if stereo flag is set in Mixer register 0Eh. Maximum sample rate is 22 kHz mono, 11 kHz stereo.
20h	1 read	Direct mode 8-bit ADC. Data is 8-bit unsigned. Firmware controlled input volume for AGC.
21h	2 read	Direct mode 16-bit ADC, returns least byte first. Data is 16-bit unsigned format. Input volume controlled by command DDh.
24h	2 writes	Start normal mode DMA for 8-bit ADC transfer. Data is transfer count - 1, least byte first. Firmware controlled input volume for AGC. Maximum sample rate is 22 kHz: use command 99h for higher rates up to 44 kHz.
25h	2 writes	Start normal mode DMA for 16-bit ADC transfer. Data is transfer count - 1, least byte first. Input volume controlled via command DDh. Maximum sample rate is 22 kHz.
2Ch		Start auto-initialize mode DMA for 8 bit ADC transfer. Block size must be previously set by command 48h. Firmware controlled input volume for AGC. Maximum sample rate is 22 kHz: use command 98h for higher rates up to 44 kHz.
2Dh		Start auto-initialize mode DMA for 16-bit ADC transfer. Block size must be previously set by command 48h. Input volume is controlled by command DDh. Maximum sample rate is 22 kHz.
30h/31h		MIDI input mode. Detects MIDI serial input data and transfers to data register, setting Data-Available flag in register 2xEh. Command 31h will also generate an interrupt request for each byte received.
		Exit MIDI input mode by executing a write to port 2xCh. The data written is ignored. A software reset will also exit this mode.
34h/35h		MIDI UART mode. Acts like commands 30h/31h, except that any data written to 2xCh will be transmitted as MIDI serial output data. The only way to exit this mode is through software reset.
38h	1 write	MIDI output. Transmit one byte.
40h	1 write	Set time constant, X, for timer used for DMA mode DAC/ADC transfers: rate = 1 MHz / (256-X) X must be less than or equal to 233. For stereo DAC, program sample rate for twice the per-channel rate.
41h	1 write	Alternate set time constant, X: rate = 1.5 MHz / (256-X)
		This command provides more accurate timing for certain rates such as 22,050. X must be less than equal to 222. For stereo DAC, program sample rate for twice the per-channel rate.
42h	1 write	Set filter clock independently of timer rate. (note that the filter clock is automatically set by commands 40h/41h) Filter clock rate: rate = 7.16E6 / (256-X)
		The relationship between the low-pass filter -3 dB point and the filter clock rate is approximately 1:82.
48h	2 writes	Set block size-1 for high speed mode and auto-init mode transfer, least byte first.

Table 10 Command Summary (Continued)

Command	Data Byte(s) Write/Read	Function
64h	2 writes	Start **ESPCM**® 4.3-bit (low compression) format DMA transfer to DAC. Data is transfer count - 1, least byte first.
65h	2 writes	Same as command 64h, except with reference byte flag.
66h	2 writes	Start **ESPCM**® 3.4-bit (medium compression) format DMA transfer to DAC. Data is transfer count - 1, least byte first.
67h	2 writes	Same as command 66h, except with reference byte flag.
6Ah	2 writes	Start **ESPCM**® 2.5-bit (high compression) format DMA transfer to DAC. Data is transfer count - 1, least byte first.
6Bh	2 writes	Same as command 6Ah, except with reference byte flag.
6Eh	2 writes	Start **ESPCM**® 4.3-bit (low compression) format ADC, compression, and DMA transfer. Data is transfer count - 1, least byte first.
6Fh	2 writes	Same as command 6Eh, except with reference byte flag.
74h	2 writes	Start ADPCM 4-bit format DMA transfer to DAC. Data is transfer count - 1, least byte first.
75h	2 writes	Same as command 74h, except with reference byte flag.
76h	2 writes	Start ADPCM 2.6-bit format DMA transfer to DAC. Data is transfer count - 1, least byte first.
77h	2 writes	Same as command 76h, except with reference byte flag.
7Ah	2 writes	Start ADPCM 2-bit format DMA transfer to DAC. Data is transfer count - 1, least byte first.
7Bh	2 writes	Same as command 7Ah, except with reference byte flag.
80h	2 writes	Generate silence period. Data is number of samples - 1.
90h		Start auto-initialize DMA 8-bit transfer to DAC. Transfer count must be previously set by command 48h.
91h		Start DMA 8-bit transfer to DAC. Transfer count must be previously set by command 48h.
98h		Start high speed mode, auto-initialize, DMA 8-bit transfer from ADC. Transfer count must be previously set by command 48h. There is no AGC. Input volume is controlled with command DDh. Maximum sample rate is 44 kHz.
99h		Start high speed mode, DMA 8-bit transfer from ADC. Transfer count must be previously set by command 48h. There is no AGC. Input volume is controlled with command DDh. Maximum sample rate is 44 kHz.
Axh, Bxh, Cxh		(where x = 0 to Fh) ES1868 Extension commands. Many of these commands are used to access the ES1868's indirect registers. For information on these registers, see the Register Descriptions.
C1h		Resume after suspend.
C6h		Enable ES1868 Extension commands Axh, Bxh. Must be issued after every reset.
C7h		Disable ES1868 Extension commands Axh, Bxh.
CEh	1 read	Read GPO0/1 Power Management register
CFh	1 write	Write GPO/1 Power Management register
D0h		Pause DMA. Internal FIFO operations will continue until the FIFO is empty (DAC transfer) or full (ADC transfer). It is not necessary to use this command to stop DMA if the transfer is completed normally and the end-of-DMA interrupt is generated.
D1h		Enable voice DAC input to mixer.
D3h		Disable voice DAC input to mixer.
D4h		Continue DMA after command D0h.
D5h	1 read	For compatibility with the ES488, always returns "1".
D6h	1 read	ES488 command not supported by ES1868. Use mixer registers instead.
D7h	1 write	ES488 command not supported by ES1868. Use mixer registers instead.

Table 10 Command Summary (Continued)

Command	Data Byte(s) Write/Read	Function
D8h	1 read	Return voice DAC enable status: 0=disabled FFh=enabled
DCh	1 read	Return current input gain, 0-15, (valid during 16-bit ADC and 8-bit “high speed mode” ADC).
DDh	1 write	Write current input gain, 0-15, (valid during 16-bit ADC and 8-bit “high speed mode” ADC).
DEh	1 read	ES488 command not supported by ES1868. Use mixer registers instead.
DFh	1 write	ES488 command not supported by ES1868. Use mixer registers instead.
E1h	2 read	Return version number high (3), followed by version number low (1). This indicates Sound Blaster Pro compatibility.
E7h	2 read	Returns ES1868 Identification bytes: 68h 8xh, where x is the version code. Sound cards not using an ES1868 will either ignore this command or perform an unknown function, in which case the sound card should be reset after this command is used. The version code, x, is less than 8 for the ES688, and greater than or equal to 8 for the ES1868.
F2h		Generate an interrupt for test purposes.
FDh		Forces power-down. Software or hardware reset. Required for wake-up.

Programming the ES1868 Enhanced Mixer

The ES1868 has a set of mixer registers that is backward compatible with the Sound Blaster Pro, but with an extended, alternate way of accessing the registers to provide for greater functionality.

Note that the mixer is read and translated by the ES1868 microprocessor, so that commands written to the mixer registers do not take effect instantly or necessarily in the same order as written.

There are 2 I/O addresses used by the mixer: 2x4h is the address port; 2x5h is the data port. In the Sound Blaster Pro, 2x4h is write only, while 2x5h is read/write. To set a mixer register, write its address to 2x4h, then write the data to 2x5h. To read the register, read from 2x5h after setting the address into 2x4h.

The mixer registers are not affected by software reset. To reset the registers to initial conditions, write any value to mixer address 0:

Write 0 to 2x4h (set mixer address to 0)

Write 0 to 2x5h (write 0 to address 0 to reset mixer)

The Sound Blaster Pro mixer volume controls are mostly 3 bits per channel. Bits 0 and 4 are always high when read. The ES1868 offers an alternative way to write each mixer register: if address bit 4 is high, all 8 bits of the register are readable and writable. This is called “Extended Access”. If address bit 4 is low, the interface is Sound Blaster Pro compatible, and bits 0 and 4 are cleared by a write, and forced high on all reads.

The Sound Blaster Pro registers that have 3 bits per channel are listed below:

Register	Function	Extended Access Register for 4 bits/Channel
04h	Voice volume	14h
22h	Master volume	32h
26h	FM volume	36h
28h	CD (Aux) volume	38h
2Eh	Line volume	3Eh

For example, if 00h is written to Sound Blaster Pro Mixer register 04h, 11h is read back because bits 0 and 4 are “stuck high” on reads. Inside the register, these bits are “stuck low,” so that writing 00h is the same as writing 11h.

A write or read to address 14h instead of 04h allows direct access to all 8 bits of this mixer register.

Extended Access to Mic Mix Volume

If Sound Blaster Compatibility Mode register address 0Ah is used to control Mic Mix Volume, only bits 2 and 1 are significant. Bit 0 is stuck high on reads and stuck low on writes. Furthermore, this is a mono control. Panning is not supported.

For Extended Access, use register address 1Ah instead. This offers 4-bits per channel for pan control of the mono microphone input to the mixer. In the ES1868 mixer, the Mic Mix Volume register is accessible in Extended Mode at address 1Ah. It is 8 bits wide, with the 4 upper bits for left volume, and the 4 lower bits for right volume as shown below:

Mic Mix Volume Register **1Ah**

7	6	5	4	3	2	1	0
Mic mix volume left				Mic mix volume right			

On reset, this register assumes the value of 00h.

Access to this register via address 0Ah is mapped as follows:

Write to 0Ah	D2=0, D1=0	Mic mix volume = 00h
	D2=0, D1=1	Mic mix volume = 55h
	D2=1, D1=0	Mic mix volume = AAh
	D2=1, D1=1	Mic mix volume = FFh
Read from 0Ah	D2 = Mic Mix Volume register bit 3	
	D1 = Mic Mix Volume register bit 2	
	D0 = 1	
	others are undefined.	

Extended Access to ADC Source Select

In Sound Blaster Compatibility Mode there are three choices for recording source, set by bits 2 and 1 of Mixer register 0Ch. Note that bit 0 is set to zero upon any write to 0Ch and set to one upon any read from 0Ch:

D2	D1	Source Selected
0	0	Microphone (default)
0	1	CD (Aux) input
1	0	Microphone
1	1	Line input

For Extended Access, use register address 1Ch to select recording from the mixer as follows:

D2	D1	D0	Source Selected
x	0	x	Microphone (default)
0	1	X	CD (Aux) input
1	1	0	Line input
1	1	1	Mixer

Programming the FIFO for DMA Playback

Data Formats

There are 8 formats available from the combination of the following 3 options:

- Mono or stereo
- 8-bit or 16-bit
- Signed or unsigned

For stereo data, the data stream always alternates channels is successive samples: first left, then right. For 16-bit data, the low byte always precedes the high byte.

Outline of Programming Steps for DMA Playback

1. Reset

   Write 3h to register 2x6h instead of 1h as in Compatibility Mode. Bit 1 high specifically clears the FIFO. The remainder of the software reset is identical to Compatibility Mode. After the reset, send command C6h to enable Extended Mode commands. Reset disables the voice input to the mixer. This is intended to mask any pops created during the setup of the DMA transfer.

2. Program Direction and Type: registers B8h, A8h, and B9h:

   Register B8h: 0 for normal DAC transfer, 4 for auto-initialize DAC transfer.

   Register A8h: read this register first to preserve the bits and modify only bits 1 and 0:
   Bits 1,0 = 1,0 Mono

   Bits 1,0 = 0,1 Stereo

   Register B9h:

   0 Single transfer DMA.
   1 Demand transfer DMA: 2 bytes per DMA request.
   2 Demand transfer DMA: 4 bytes per DMA request.

3. Clocks and Counters: registers A1h, A2h, A4h and A5h:

   Register A1h = Sample Rate Clock Divider
   Register A2h = Filter Clock Divider
   Registers A4h/A5h = DMA Counter Reload register low/high byte, 2's complement.

4. Initialize and Configure DACs: registers B6h and B7h

   The DACs must be configured and initialized with a command sequence depending on the data format shown in Table 11.

5. Enable/Select DMA Channel and IRQ Channel: registers B1h and B2h:

   Register B1h: Interrupt configuration register.
   Make sure bits 4 and 6 are high, clear bits 7 and 5.

   Register B2h: DRQ configuration register.
   Make sure bits 4 and 6 are high, clear bits 7 and 5.

6. Configure system interrupt controller and DMA controller.

Table 11 Command Sequences for DMA Playback

Mono	Stereo	8-bits	16-bits	Unsigned	Signed	Sequence
X		X		X		Reg B6h = 80h, Reg B7h = 51h, Reg B7h = D0h
X		X			X	Reg B6h = 00h, Reg B7h = 71h, Reg B7h = F0h
X			X	X		Reg B6h = 80h, Reg B7h = 51h, Reg B7h = D4h
X			X		X	Reg B6h = 00h, Reg B7h = 71h, Reg B7h = F4h
	X	X		X		Reg B6h = 80h, Reg B7h = 51h, Reg B7h = 98h
	X	X			X	Reg B6h = 00h, Reg B7h = 71h, Reg B7h = B8h
	X		X	X		Reg B6h = 80h, Reg B7h = 51h, Reg B7h = 9Ch
	X		X		X	Reg B6h = 00h, Reg B7h = 71h, Reg B7h = BCh

7. Recommended: delay approximately 100 milliseconds before enabling voice input to mixer.

8. Enable voice to mixer with command D1h.
9. To Start DMA:

   Set bit 0 of register B8h high while preserving all other bits.
10. During DMA:

    For auto-initialize transfers, do not send any commands to the ES1868 at interrupt time, except for reading 2xEh to clear the interrupt request.

    For normal mode, initialize the system DMA controller with the address and count of the next block to transfer. Update the ES1868 Transfer Count registers if the count is changed. To start the next transfer, clear bit 0 of register B8h, then set it high again.

    To stop a DMA transaction in progress, clear bit 0 of register B8h.
    To stop a DMA transaction after the current auto-initialize block is finished, clear bit 2 of register B8h, wait for the interrupt, and then clear bit 0 of the B8h.
11. After DMA is finished, restore the system interrupt controller and DMA controller to their idle state. Monitor the FIFO Empty status flag in register 2xCh to be sure data transfer is completed. A delay of 25 milliseconds is required to let the filter outputs settle to DC levels, then mute the Voice input to mixer with command D3h.
12. Finally, issue another software reset to the ES1868 to initialize the appropriate registers.

Programming the FIFO for DMA Record

Data Formats

There are 8 formats available from the combination of the following 3 options:

- Mono or stereo
- 8-bit or 16-bit
- Signed or Unsigned

For stereo data, the data stream always alternates channels is successive samples: first left, then right. For 16-bit data, the low byte always precedes the high byte.

No Automatic Gain Control for 8-bit Recordings

In Extended Mode, there is no Automatic Gain Control (AGC) performed while recording. If AGC is necessary, use 16-bit recordings and perform AGC in system software.

Outline of Programming Steps for DMA Recording

1. Reset: Write 3h to register 2x6h instead of 1h as in Compatibility Mode. Bit 1 high specifically clears the FIFO. The remainder of the software reset is identical to Compatibility Mode. After the reset, send command C6h to enable Extended Mode commands.
2. Select the input source using the Mixer register 0Ch.
3. Program Input Volume: register B4h
4. Program Direction and Type: registers B8h, A8h

   Register B8h: 0Ah for normal ADC transfer, 0Eh for auto-initialize ADC transfer.

   At this point the direction of the analog circuits becomes ADC rather than DAC. Unless recording monitor is enabled, there will be no output from AOUT_L or AOUT_R until the direction is restored to DAC.

   Register A8h: read this register first to preserve the bits and modify only bits 3, 1, and 0:

   Bits 1,0 = 1,0 for mono and 0,1 for stereo

   Bit 3 = 0 Disable Record Monitor for now

   Register B9h: 0: Single Transfer DMA
   1: Demand Transfer, 2 bytes per DMA request
   2: Demand Transfer, 4 bytes per DMA request
5. Clocks and Counters: registers A1h, A2h, A4h and A5h

   Register A1h = Sample Rate Clock Divider. Set bit 7 high for sample rates greater than 22 kHz.

   Register A2h = Filter Clock Divider

   Registers A4h/A5h = DMA Counter Reload register low/high byte, 2's complement
6. Delay 100 milliseconds to allow the analog circuits to settle.
7. Enable Record Monitor if desired:

   Register A8h Bit 3=1: Enable Record Monitor (optional)
8. Initialize and Configure ADC: register B7h

The ADCs must be configured and initialized with a command sequence depending on the data format shown in Table 12:

Table 12 Command Sequence for DMA Record

Mono	Stereo	8-bits	16-bits	Unsigned	Signed	Sequence
X		X		X		Reg B7h = 51h, Reg B7h = D0h
X		X			X	Reg B7h = 71h, Reg B7h = F0h
X			X	X		Reg B7h = 51h, Reg B7h = D4h
X			X		X	Reg B7h = 71h, Reg B7h = F4h
	X	X		X		Reg B7h = 51h, Reg B7h = 98h
	X	X			X	Reg B7h = 71h, Reg B7h = B8h
	X		X	X		Reg B7h = 51h, Reg B7h = 9Ch
	X		X		X	Reg B7h = 71h, Reg B7h = BCh

9. Enable/Select DMA Channel and IRQ Channel: registers B1h and B2h:

   Register B1h: Interrupt Configuration register.
   Verify that bits 4 and 6 are high. Clear bits 7 and 5.

   Register B2h: DRQ Configuration register:
   Verify that bits 4 and 6 are high. Clear bits 7 and 5.

10. Configure system interrupt controller and DMA controller.
11. To Start DMA: Set bit 0 of register B8h high. Leave other bits unchanged.
12. During DMA:

    For auto-initialize transfers, do not send any commands to the ES1868 at interrupt time, except for reading 2xEh to clear the interrupt request.

    For normal mode, initialize the system DMA controller with the address and count of the next block to transfer. Update the ES1868 Transfer Count registers if the count is changed. To start the next transfer, clear bit 0 of register B8h, then set it high again.

    To stop a DMA transaction in progress, clear bit 0 of register B8h.

    To stop a DMA transaction after the current auto-initialize block is finished, clear bit 2 of register B8h, wait for the interrupt, and then clear bit 0 of the B8h.

13. After DMA is finished, restore the system interrupt controller and DMA controller to their idle state.
14. Finally, issue another software reset to the ES1868 to initialize the appropriate registers. This will return the ES1868 to the DAC direction and turn off the record monitor.

Programming the FIFO for I/O Block Transfer

For some applications, DMA is not suitable or available for data transfer, and it is not possible to take exclusive control of the system for DAC and ADC transfers. In these situations, use I/O block transfers within an interrupt handler. The REP OUTSB instruction of the 80x86 family transfers data from memory to an I/O port specified by the DX register. The REP INSB instruction is the complementary function. Use ES1868 port 2xFh for block transfers.

I/O transfers to FIFO are nearly identical to the DMA process described above, except that an I/O access to port 2xFh replaces the DMA cycle. Some differences are described here.

The DRQ control register B2h bits 7:5 should all be low. This is because no actual DRQ/DACKB cycle is needed.

The IRQ control register B1h must have bit 5 high to enable an interrupt on FIFO half-empty transitions. Bit 6 should be low to avoid an interrupt from the DMA counter.

To program in this mode it is useful to understand how the FIFO Half-Empty flag generates an interrupt request: An interrupt request is generated on the rising edge of the FIFO Half-Empty flag. This flag can be polled by reading port 2xCh. The meaning of this flag depends on the direction of the transfer:

DAC FIFOHE flag is set high if 0-127 bytes in FIFO

ADC FIFOHE flag is set high if 128-256 bytes in FIFO

For DAC operations an interrupt request is generated when the number of bytes in the FIFO changes from >=128 to < 128. This indicates to the system processor that 128 bytes can be safely transferred without over-filling the FIFO. Before the first interrupt can be generated, the FIFO needs to be primed, or filled, with more than 128 bytes. Keep in mind that data may be taken out of the FIFO while it is being filled by the system processor. If that is the case, there may never be >= 128 bytes in the FIFO unless somewhat more than 128 bytes is transferred. A solution is to poll the ES1868 FIFOHE flag to be sure it goes low in the interrupt handler (or when priming the FIFO) and perhaps send a second block of 128 bytes.

For ADC, the interrupt request is generated when the number of bytes in the FIFO changes from < 128 to >= 128, indicating that the system processor can safely read 128 bytes from the FIFO. Before the first interrupt can be generated, the FIFO should be emptied (or mostly so) by reading from 2xFh and polling the FIFOHE flag. Its not safe to indiscriminately use the FIFO reset bit 1 of port 2x6h to clear the FIFO, because it may get ADC data out-of-sync

As in DMA mode, bit 0 of register B8h enables transfers between the system and the FIFO inside the ES1868.

Note: The ES1868 is designed for I/O block transfer up to a ISA bus speed of 8.33 MHz.

PORTS

Port Addresses and Functions Summarized

Table 13 lists ES1868 port addresses and the function assigned to each port and its bits.

Table 13 Port Addresses and Functions

Port	Read/write	Bit	Function
0E0h, 0E1h, 0F9h, 0FBh			Used by Software Address Configuration, if enabled
201h	Read/write		Decoded along with IORB and IOWB to access internal joystick port
2x0h-2x3h	Read/write		20-voice FM synthesizer. Address and data registers.
2x4h	Read/write		Mixer Address register (port for address of mixer indirect registers)
2x5h	Read/write		Mixer Data register (port for data to/from mixer indirect registers).
2x6h	Write	0	1 = hold ES1868 in reset 0 = release ES1868 from reset
		1	1 = hold ES1868 FIFO in reset 0 = release ES1868 FIFO from reset Note: Bit 1 is “don’t care” for Compatibility Mode.
	Read		Activity flags and other status for power management.
2x7h	Read/write		Power Management register.
2x8h-2x9h	Read/write		11-voice FM synthesizer. Address and data registers.
2xAh	Read-only		Input data from read buffer for Command/Data I/O. Poll bit 7 of port 2xEh to test whether the read buffer contents are valid.
2xCh	Write		Write data to write buffer for command/data I/O. Sets Write-Buffer-Not-Available flag until data is processed by the ES1868.
	Read	7	1 = write buffer not available or ES1868 busy. 0 = write buffer is available and ES1868 not busy.
		6	same as bit 7 of port 2xEh.
		5	1 = Extended Mode FIFO full (256 bytes loaded)
		4	1 = Extended Mode FIFO empty (0 bytes loaded)
		3	1 = FIFO Half-Empty, Extended Mode flag.
		2	1 = ES1868 processor generated an interrupt request (e.g., from Compatibility Mode DMA complete)
		1	1 = Interrupt request generated by FIFO Half-Empty flag change. Used by programmed I/O interface to FIFO in Extended Mode.
		0	1 = Interrupt request generated by DMA counter overflow in Extended Mode.
2xEh	Read-only	7	1 = Data available in read buffer. A read from port 2xEh will reset any IRQ request.
2xFh	Read/write		Address for I/O access to FIFO in Extended Mode.
3x0h-3x1h	Read/write		MPU-401 port (x=0,1,2, or 3) if enabled.
388h-38Bh	Read/write		Same as 2x0h-2x3h, i.e. 20-voice FM synthesizer

Port Descriptions

2x6H (Write)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FIFO reset	S/W reset

2x6H (Read)

7	6	5	4	3	2	1	0
Act flag 2	Act flag 1	Act flag 0	Serial act	0 if power -down	MIDI mode	FIFO reset	S/W reset

Reading port 2x6h returns the following information:

Bits 7:5 Activity flags: These three bits are flags that are reset low by certain I/O activity. They are all set high each time that this port, 2x6h, is read:

Bit 7 Activity Flag 2: set low by any read/write of an FM port or MPU-401 port:

2x8h-2x9h, 388h-389h, 3x0h-3x1h.

Bit 6 Activity Flag 1: set low by:

read 2xCh

read 2xEh

Bit 5 Activity Flag 0: set low by any DMA read/write or the following:

read/write 2x2h-2x3h

write 2x6h

read 2xAh

write 2xCh

Bit 4 1 = Serial activity flag. High if DSP serial mode is enabled (SE input pin high or bit 7 of Mixer Extension register 48h is high), or, if an external ES689/ES690 is using MCLK/MSD to drive the FM DACs.

Bit 3 0 = The ES1868 digital section is currently powered down. In this state the power to the analog section is controlled by bit 3 of port 2x7h.

Bit 2 1 = The ES1868 is processing a MIDI command 30h, 31h, 34h, or 35h. In this mode the ES1868 is monitoring serial input. Powering down may cause loss of data.

Note that the ES1868 does not automatically wake up on serial input on the MSI pin.

Bit 1 FIFO Reset register

Bit 0 Software Reset register

Power Management Register 2x7H (Read/Write)

7	6	5	4	3	2	1	0
Suspend request	x	1:Reset FM synth	0	Analog stays on	power-down request	GPO 1	GPO 0

Reading or writing port 2x7h will not automatically wake up the ES1868.

Bit 7 Suspend request. Pulse high, then low, to request suspend.

Bit 6 Unknown (read only).

Bit 5 1 = FM synthesizer reset
0 = Release FM synthesizer reset

Bit 4 Reserved, should be set low.

Bit 3 1 = set Analog_stays_on
0 = clear Analog_stays_on

Bit 2 Power-down request. Pulse high, then low, to request power-down.

Bit 1 1 = Set GPO1 = 1 (hardware reset condition)
0 = Clear GPO1 = 0

Bit 0 1 = Set GPO0 = 1
0 = Clear GPO0 = 0 (hardware reset condition)

REGISTER OVERVIEW

This section provides an overview of, and general information about, ES1868 registers.

Register Types

Types of Register Access

There are two types of access to registers in the ES1868. *Direct* registers can be accessed by a read or write directly to the register address. *Indirect* registers can be accessed only by reading or writing commands and data to another register, generally through a port.

Types of Registers

There are three general categories of registers. These are:

- Sound Blaster Compatibility Registers
  These provide Sound Blaster functions for the ES1868.
- Mixer Control Extension Registers
  These control ESS extensions to the mixer architecture, for greater capability.
- General Control Extension Registers
  These control general operating functions such as IRQ handling, and functions ESS has added to enhance the capabilities of this chip.

Sound Blaster Compatibility Registers

Sound Blaster Compatible Mixer Registers

Sound Blaster Compatibility registers are direct registers. They are listed in Table 14.

Table 14 Sound Blaster Compatibility Registers

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Description
00h	Write: reset mixer								Mixer reset
04h	Voice volume left			X	Voice volume right			X	
0Ah	X	X	X	X	X	Mic mix volume		X	
0Ch	X	X	F1 *	X	F0 *	ADC source		X	see note for F0, F1
0Eh	X	X	F2 *	X	X	X	Stereo	X	see note for F2
22h	Master volume left			X	Master volume right			X	
26h	FM volume left			X	FM volume right			X	Synthesizer volume
28h	CD (AuxA) volume left			X	CD (AuxA) volume right			X	CD volume control
2Eh	Line volume left			X	Line volume right			X	

* Sound Blaster Filter Control bits F2, F1, and F0 have no equivalent function in the ES1868 and are ignored.

Mixer Control Extension Registers

Mixer Control Extension Registers Summarized

The Mixer Control Extension Registers are indirect registers. They are accessed by writing to or reading from ports 2x4h and 2x5h. They are listed in Table 15.

Table 15 ESS Mixer Registers Summary

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Remark
1Ah	Mic mix volume left				Mic mix volume right				Mic mix volume
40h	ES1868 identification value								Read-only
42h	Input override	Mic 0 dB	IS1	IS0	Input volume				Serial mode input control
44h	Output override	Output signal			Output volume				Serial mode output control
46h	Analog control override	0	Left ADC	Right ADC	AC1	AC0	FDXO enable	FDXI enable	Serial mode miscellaneous analog control
48h	SW SE	2's comp	Serial reset	Enable ES689/ ES690 Intfc	Active low sync	0	0	0	Serial mode miscellaneous control
4Ch	Filter override	0	0	0	2's complement filter divider				Serial mode filter divider control
4Eh	TX SRC1	TX SRC0	TX 16/8	TX stereo/ mono	RX SRC1	RX SRC0	RX 16/8	RX stereo/ mono	Serial mode format/source/ target control
64h	X	MPU-401 int mask	X	Read-only HMV int request	X	X	HMV int mask	Disable SB Pro master volume control	Master volume control
66h	Clear hardware volume interrupt request								Write-only
74h	Two's complement transfer count – low byte								Second DMA transfer count reload register
76h	Two's complement transfer count – high byte								
78h	Single/demand transfer		0	1: Auto-initialize	0	0	Enable second channel DMA	Enable full-duplex mode	Second DMA control 1
7Ah	Interrupt req latch		0	0	0	Data sign	Stereo /Mono	16-bit /8-bit	Second DMA control 2

Mixer Control Extension Register Descriptions

Mic Mix Volume **1Ah**

7	6	5	4	3	2	1	0
Mic mix volume left				Mic mix volume right			

On reset, this register assumes the value of 00h.

Serial Mode Input Control **42h**

7	6	5	4	3	2	1	0
Input override	Mic 0 dB	IS1	IS0	Input volume			

Bit 7 1 = IS1/IS0 and INPUT VOLUME replace normal values as programmed by the system application when the ES1868 is in Serial Mode. Note input volume is mono, and both channels will get this value.

0 = IS1/IS0 and INPUT VOLUME are unchanged during Serial Mode.

Bit 6 1 = the 26 dB microphone preamp is bypassed during Serial Mode (if bit 7 is high).

Bits 5:4 IS1/IS0 select the input source during Serial Mode (if bit 7 is high). These values override the normal mixer settings as shown in the following:

IS1	IS0	Input Source
0	0	Line
0	1	AuxA (CD)
1	0	Mic
1	1	Mixer

Bits 3:0 Input volume. If bit 7 is high during Serial Mode, this value overrides the input volume settings set via command B4h.

Serial Mode Output Control **44h**

7	6	5	4	3	2	1	0
Output override	Output signal			Output volume			

Bit 7 1 = Output Volume during Serial Mode is taken from this register rather than from the normal Mixer Master Volume register. Note that the Output Signal control is always in force during Serial Mode regardless of the state of this bit.

Bits 6:4 These bits control the signal routed to the speaker outputs AOUT_L and AOUT_R.

BITS			SIGNAL
6	5	4	
0	0	0	Mute
0	0	1	FDXI monitor in both channels
0	1	0	FDXO monitor in both channels
0	1	1	FDXI monitor in left channel, FDXO in right channel
1	0	0	Mixer output
1	0	1	Mixer output - Wave (Wave input muted)
1	1	0	Mixer output - Wave - FM
1	1	1	Reserved

Bits 3:0 Output volume. Replaces normal mixer Master Volume setting if bit 7 is high during Serial Mode.

Serial Mode Miscellaneous Analog Control **46h**

7	6	5	4	3	2	1	0
Analog control override	0	Left ADC	Right ADC	AC1	AC0	FDXO enable	FDXI

Bit 7 1 = bits 6:0 of this register take effect during Serial Mode.
0 = bits 6:0 do not ever take effect.

Bit 6 Reserved. Should be set to 0.

Bit 5 1 = Left channel combined ADC and DAC is in ADC mode.
0 = Left channel combined ADC and DAC is in DAC mode.

Bit 4 1 = Right channel combined ADC and DAC is in ADC mode.
0 = Right channel combined ADC and DAC is in DAC mode.

Bit 3:2 Analog Control bits 1:0. These special control signals control interconnections in the analog circuitry. They should be set appropriately for the application as follows:

Application	AC1	AC0
Stereo wave playback or record	0	0
Mono wave playback or record	1	1
Full-duplex (mono record and playback)	1	0

Bit 1 1 = Enables FDXO output connection to output pin FOUT_R (right channel filter output)
0 = FDXO has 50K pull-up to CMR.

Bit 0 1 = Enables FDXI input connection to left channel filter input and thus to the input of the left channel ADC.
0 = FDXI input has 50K pull-up to CMR. The left channel filter input and ADC comes from input volume stage as usual.

Serial Mode Miscellaneous Control 48h

7	6	5	4	3	2	1	0
SW SE	2's comp	Serial reset	Enable ES689/ ES690 intfc	Active low sync	0	0	0

Bit 7 1 = Force Serial Mode regardless of state of SE pin.
0 = Serial Mode controlled by SE pin.

Bit 6 1 = Data format is 2's complement.
0 = Data format is unsigned.

Bit 5 1 = Reset serial register left/right toggle flags.
0 = Release reset.

Serial Reset also inhibits FDXO connection to FOUT_R and "zeros" all shift registers.

Bit 4 1 = Enable ES689/ES690 to acquire FM DACs when serial activity present on pins MCLK and MSD.
0 = Prevent ES689/ES690 from acquiring FM DACs.

Bit 3 1 = Sync pulses (FSR, FSX) are active-low.

Bit 2 Reserved. Always write 0.

Bit 1 Reserved. Always write 0.

Bit 0 Reserved. Always write 0.

Serial Mode Filter Divider 4Ch

7	6	5	4	3	2	1	0
Filter override	0	0	0	2's complement filter divider			

This register controls the filter clock rate during Serial Mode.

Bit 7 1 = During Serial Mode, the filter clock is generated by dividing down the serial clock.
0 = During Serial Mode, the filter clock is generated as usual.

Bit 6 Reserved. Always write 0.

Bit 5 Reserved. Always write 0.

Bit 4 Reserved. Always write 0.

Bit 3:0 Bits 3:0 are a 2's complement value that divides down the serial clock. The ratio of the filter -3 dB frequency to the filter clock is approximately 1:41.

Examples:

02h (-14) External Serial Clock 2.048 MHz / 14 / 41 = 3568 Hz for 8000 Hz Sample Rate.

0Eh (-2) Internal Serial Clock 1.591 MHz / 2 / 41 = 19.4 kHz for 44,100 Sample Rate. Note that the sample rate divider is an integer multiple of the filter divide for 44,100, which gives maximum performance of DACs and ADCs.

Serial Mode Format/Source/Target 4Eh

7	6	5	4	3	2	1	0
TX SRC1	TX SRC0	TX 16/8	TX stereo/ mono	RX SRC1	RX SRC0	RX 16/8	RX stereo/ mono

Bits 7:6 Transmit register source

BIT		Source
7	6	
0	0	None: Transmit Register held at "Zero" code
0	1	FIFO
1	0	Left ADC or stereo ADC transmission
1	1	Right ADC

Bit 5 1 = Transmit length is 16 bits, unsigned
0 = Transmit length is 8 bits, unsigned

Bit 4 1 = Transmit mode is stereo. Left and right channels alternate, with left channel data preceding right channel data.
0 = Transmit mode is mono.

Bits 3:2 Receive Register Target

BIT		Target
3	2	
0	0	None: Receive Register held at "Zero" code
0	1	FIFO
1	0	DAC (if mono, right channel receives data, left channel receives complement of data)
1	1	FM DAC (if mono, right channel receives data, left channel receives complement of data)

Bit 1 1 = Receive length is 16 bits, unsigned
0 = Receive length is 8 bits, unsigned

Bit 0 1 = Receive mode is stereo. Left and right channels alternate, with left channel data preceding right channel data.
0 = Receive mode is mono.

Left Master Volume Counter Value **60h**

7	6	5	4	3	2	1	0
0	1: MUTE	Left master volume					

Right Master Volume Counter Value **62h**

7	6	5	4	3	2	1	0
0	1: MUTE	Right master volume					

Master Volume Control **64h**

7	6	5	4	3	2	1	0
X	MPU-401 int mask	X	Read-only HMV int request	X	X	HMV int mask	1: Disable SB Pro master vol control

Bit 6 This bit is AND'ed with the MPU-401 interrupt request. If it is low, the MPU-401 interrupt request stays low. This bit is cleared by hardware reset.

Bit 4 Read only interrupt request from hardware volume event.

Bit 1 This bit is AND'ed with the hardware volume interrupt request before being OR'd with the first channel audio interrupt request. If this bit is low, the hardware volume interrupt request does not get OR'd with the first channel audio interrupt request. This bit is cleared by hardware reset.

Bit 0 When low, a write to the Sound Blaster Pro master volume register will be translated into a write to the hardware master volume counters, Mixer registers 60h and 62h. If high, the Sound Blaster Pro master volume registers are, in effect, read-only. This bit is cleared by hardware reset.

Clear Hardware Volume Interrupt Request **66h**

Clear Hardware Master Control

Any write to this register resets the hardware volume interrupt request.

Second DMA Transfer Count Reload Register **74h**

7	6	5	4	3	2	1	0
2's complement transfer count - low byte							

Second DMA Transfer Count Reload Register **76h**

7	6	5	4	3	2	1	0
2's complement transfer count - high byte							

Second DMA Control **78h**

7	6	5	4	3	2	1	0
		0		0	0		

Bit 7:6 0 0 Single Transfer: 1 DACK per DRQ
0 1 Demand Transfer: 2 DACKs per DRQ
1 0 Demand Transfer: 4 DACKs per DRQ
1 1 Demand Transfer: 8 DACKs per DRQ

Bit 5 Reserved. Write 0.

Bit 4 1 = Auto-initialize mode. After the transfer counter rolls over to 0, it is automatically reloaded and DMA continues. The second channel interrupt flag will be set high.

0 = Normal mode. After the transfer counter rolls over to 0, it is reloaded but DMA stops. Bit 1 of this register is cleared. The second channel interrupt flag will be set high.

Bits 3:2 Reserved. Write 0.

Bit 1 When high, second channel DMA is enabled. This bit is cleared when the transfer counter rolls over to 0 if not in auto-initialize mode.

Bit 0 When high, full-duplex mode is enabled. The left channel is used for recording, and the right channel is used for playback.

This register is reset to all zero by hardware or software reset via bit 0 of port 2x6h.

Second DMA Control 2 **7Ah**

7	6	5	4	3	2	1	0
		0	0	0	0		

This register is reset to zero by hardware or software reset.

Bit 7 Second DMA channel interrupt request latch. This latch is set high when the DMA counter rolls over to zero, or when a 1 is written to this bit. The latch is cleared by writing a zero to this bit, or by hardware or software reset.

Bit 6 This bit is AND'ed with bit 7 to produce the second DMA channel interrupt request.

Bit 5:3 Reserved, write 0.

Bit 2 1 = Data is in signed, 2's complement format.
0 = Unsigned data

Bit 1 1 = Stereo data. This format is reserved for Interleave Mode when using the DSP serial interface.
0 = mono data.

Bit 0 1 = 16-bit samples.
0 = 8-bit samples.

General Control Extension Registers

General Control Extension Registers Summarized

The General Control Extension Registers are indirect registers. They are accessed by writing to or reading from ports 2xCh and 2xEh. They are listed in Table 16.

Table 16 General Control Extension Registers

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Description
A1h	1: > 22 kHz 0: <= 22 kHz	Extended Mode sample rate divider							S/W reset, unknown
A2h	Filter clock divider								S/W reset, setup for 8 kHz sampling
A4h	DMA transfer counter reload – low byte								
A5h	DMA transfer counter reload – high byte								
A9H	Reserved					Enable mic preamp	Reserved		
B1h	Processor IRQ	Enable IRQ on DMA cntr ovf	Enable IRQ on FIFOHE change	x					Interrupt Control
B2h	Processor DRQ	Enable DRQ for Ext DMA	Enable DRQ for Comp Mode DMA	x					DMA Control
BAh	0	Enable SR Adjust	Disable time delay on analog wake-up	Reserved: write 0					
BCh	FM DAC vol 1	FM DAC vol 0	1	1	0	1	1	0	

General Control Extension Register Descriptions

Extended Mode Sample Rate Generator **A1h**

7	6	5	4	3	2	1	0
1: > 22 kHz 0: <= 22 kHz	Sample rate divider						

This register should be programmed for the sample rate for all DAC and ADC operations in Extended Mode.

The clock source for sample rate generator is 397.7 kHz if bit 7 is 0 and 795.5 kHz if bit 7 is 1.

The sample rate is determined by the two's complement divider in bits 7:0:

Sample_Rate = 397.7 kHz / (128-x) if bit 7 = 0.
= 795.5 kHz / (256-x) if bit 7 = 1.
where: x = value in bits 7:0 of register A1h.

Filter Divider **A2h**

7	6	5	4	3	2	1	0
Filter clock divider							

This register controls the low-pass frequency of the switch-capacitor filters inside the ES1878. Generally, the filter roll-off should be positioned at 80% - 90% of the Sample_Rate/ 2 frequency. The ratio of the roll-off frequency to the filter clock frequency is 1:82. In other words, first determine the desired roll-off frequency by taking 80% of the Sample_Rate divided by 2, then multiply by 82 to find the desired Filter Clock frequency. Use the formula below to determine the closest divider:

Filter_Clock_Frequency = 7.16 MHz / (256-Filter_Divider_Register)

DMA Transfer Count Reload Register **A4h**

7	6	5	4	3	2	1	0
DMA transfer counter reload – low byte							

On reset, this register assumes the value of 00h.

DMA Transfer Count Reload Register **A5h**

7	6	5	4	3	2	1	0
DMA transfer counter reload – high byte							

On reset, this register assumes the value of F8h.

The FIFO control logic of the ES1878 has a 16-bit counter for controlling transfers to and from the FIFO. These registers are the reload value for that counter which is the value that gets copied into the counter after each overflow (plus at the beginning of the initial DMA transfer). The counter will be incremented after each successful byte is transferred via DMA. Since the counter counts up towards FFFFh and then overflows, the reload value is in 2's complement form.

For Auto-Initialize DMA, the counter is used to generate interrupt requests to the system processor: in this mode DMA continues indefinitely as far as the ES1878 is concerned. In a typical application the counter is programmed to be one-half of the DMA buffer maintained by the system processor. In this case an interrupt is generated whenever DMA switches from one half of the circular buffer to the other.

For Normal Mode DMA, DMA requests will be halted at the time that the counter overflows, until a new DMA transfer is commanded by the system processor. Again, an interrupt request will be generated to the system processor if bit 6 of register B1 is set high.

Mic Preamp **A9h**

7	6	5	4	3	2	1	0
Reserved					Enable mic preamp	Reserved	

Bit 2, if set high, enables +26 dB gain in the microphone preamp. If set low, the microphone preamp has no gain (0 dB). This bit is set high by hardware reset.

Note: All other bits must first be read and preserved when writing to this register.

Interrupt Control Register **B1h**

7	6	5	4	3	2	1	0
Processor IRQ	Enable IRQ on DMA cntr ovf	Enable IRQ on FIFOHE change	x				

Bit 7 Processor IRQ. Reserved for Compatibility Mode. Should be left zero for Extended Mode.

Bit 6 Should be set high to receive interrupts for each overflow of the ES1868 DMA counter in Extended Mode.

Bit 5 Should be set high to receive interrupts for FIFO Half-Empty transitions when doing block I/O to/from the FIFO in Extended Mode.

Bit 4 Bit 4 of Extended register B1h is don't-care, not the interrupt enable control. The audio device activate bit serves the purpose of enabling the interrupt pin.

Bit 3:0 Read-only. They decode the selected interrupt number for the first audio interrupt as follows:

Bits				Audio 1 Interrupt
3	2	1	0	
0	0	0	0	2, 9, all others
0	1	0	1	5
1	0	1	0	7
1	1	1	1	10

DMA Control Register **B2h**

7	6	5	4	3	2	1	0
Processor DRQ	Enable DRQ for Extended DMA	Enable DRQ for Comp Mode DMA	x				

Bit 7 Reserved for Compatibility Mode; should be left zero for Extended Mode.

Bit 6 1 = Enable DRQ outputs and DACKB inputs for DMA transfers in Extended Mode.
0 = Enable block I/O to/from the FIFO in Extended Mode.

Bit 5 Reserved for Compatibility Mode; should be left zero for Extended Mode.

Bit 4 Bit 4 of register B2h is don't-care. The DRQ lines always drive there is no enable). If neither bit 6 or 5 are set high, the 1st audio DRQ is always low.

Bits 3:0 Read-only. The selected DMA channel number for the first audio DMA channel are decoded to set register B2h bits 3:2, and 1:0 as follows:

Bits				Audio 1 DMA
3	2	1	0	
0	1	0	1	0
1	0	1	0	1
1	1	1	1	3
0	0	0	0	all others

BAh

7	6	5	4 3 2 1 0
0	Enable SR ADJ	1:Disable time delay on analog wake-up	Reserved: write 0

Bit 6 The ES1868 includes this feature of the ES1888 that adjusts the sample rates for more accuracy.
1= Cause the 14.31818 MHz cock to be adjusted slightly to make the 44.1 kHz sample rate (and integral divisions of that rate) nearly exact.
This bit is cleared by hardware reset.

Bit 5 Normally, the AOUT_L and AOUT_R pins are muted for 100 milliseconds ± 20 milliseconds after hardware reset or after the analog subsystems wake from power-down. This delay can be disabled by setting bit 5. This bit is cleared by hardware reset.

BCh

7	6	5	4	3	2	1	0
FM DAC volume 1	FM DAC volume 0	1	1	0	1	1	0

Bit 7:6 See table below:

BIT 7	BIT 6	FM DAC Level
VOL1	VOL0	
0	0	-1.5 dB: recommended level if ES689/ES690 shares FM DAC
0	1	+1.5 dB
1	0	0 dB (hardware reset default)
1	1	-3 dB

Bit 5:0 For proper operation must be set to value of 110110 as shown.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Value
Analog supply voltage range	VDDA	-0.3 to 7.0 V
Digital supply voltage range	VDDD	-0.3 to 7.0 V
Input voltage	VIN	-0.3 to 7.0 V
Operating temperature range	TA	0 to 70 °C
Storage temperature range	TSTG	-50 to 125 °C

Thermal Characteristics

The ES1868 is designed to operate at temperatures between 0 °C and less than +85 °C.

WARNING: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the Operating Conditions is not recommended, and extended exposure beyond the Operating Conditions may affect device reliability.

Operating Conditions

Digital supply voltage. . . . . 3.0 V to +5.50 V

Analog supply voltage . . . . . 4.75 V to +5.25 V

DC Electrical Characteristics

Table 17 Digital Characteristics

(VDDD = 5.0 V ± 10%; TA = 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit (conditions)
VIH1	Input high voltage: all inputs except XI	2.0 V			VDDD = min
VIH2	Input high voltage: XI	3.0 V			VDDD = min
VIL	Input low voltage		0.8 V		VDDD = max
VOL1	Output low voltage: all outputs except D[7:0], IRQ(A-F), DRQ(A-D)		0.4 V		IOL = 4mA, VDDD = min
VOH1	Output high voltage: all outputs except D[7:0], IRQ(A-F), DRQ(A-D)	2.4 V			IOH = -3mA, VDDD = max
VOL2	Output low voltage:D[7:0], IRQ(A-F), DRQ(A-D)		0.4 V		IOL = 16mA, VDDD = min
VOH2	Output high voltage: D[7:0], IRQ(A-F), DRQ(A-D)	2.4 V			IOH = -12mA, VDDD = max

Table 18 Analog Characteristics

(VDDD = 5.0 V ± 5%; TA = 25 °C)

Pins	Parameter	Min	Typ	Max	Units
CMR, VREF	Reference voltage		2.25		volts
LINE_L, LINE_R, AUXA_L, AUXA_R, AUXB_L, AUXB_R, MIC	Input Impedance	30k	100k		ohms
CIN_L, CIN_R		35k	50k	65k	ohms
FOUT_L, FOUT_R	Output impedance	3.5k	5k	6.5k	ohms
AOUT_L, AOUT_R max load for full-scale output range			5k		ohms
MIC	Input voltage range	10		125	mVp-p
LINE_L, LINE_R, AUXA_L, AUXA_R, AUXB_L, AUXB_R		0.5		VDDA-1.0	volts
AOUT_L, AOUT_R full-scale output range	Output voltage range	0.5		VDDA-1.0	volts
MIC	Mic preamp gain		26		decibels

TIMING DIAGRAMS

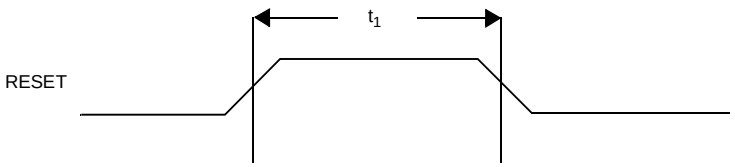


Figure 19 Reset Timing

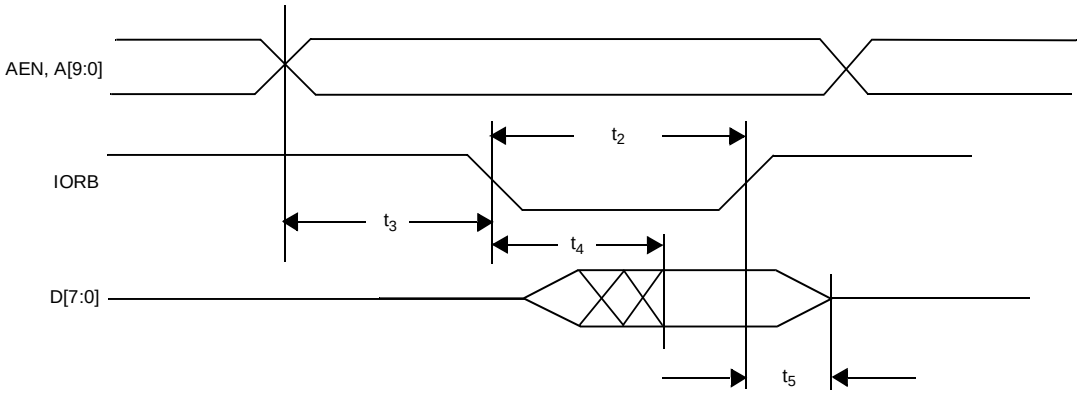


Figure 20 I/O Read Cycle

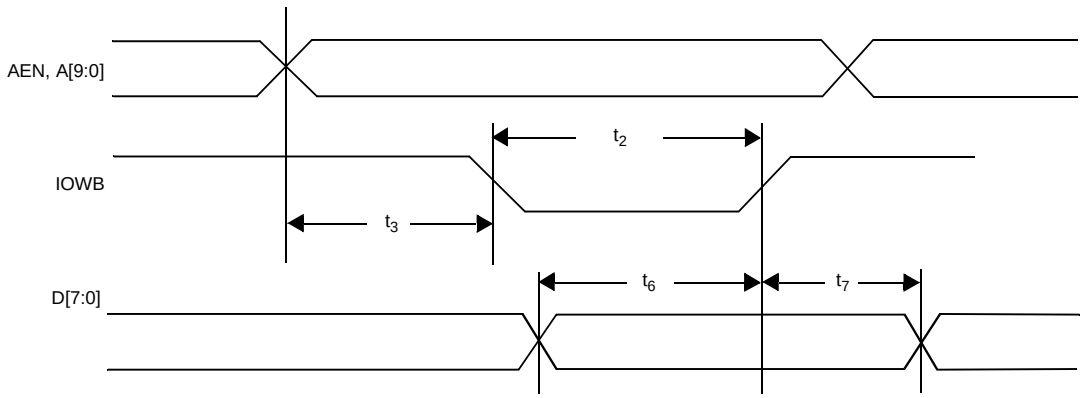


Figure 21 I/O Write Cycle

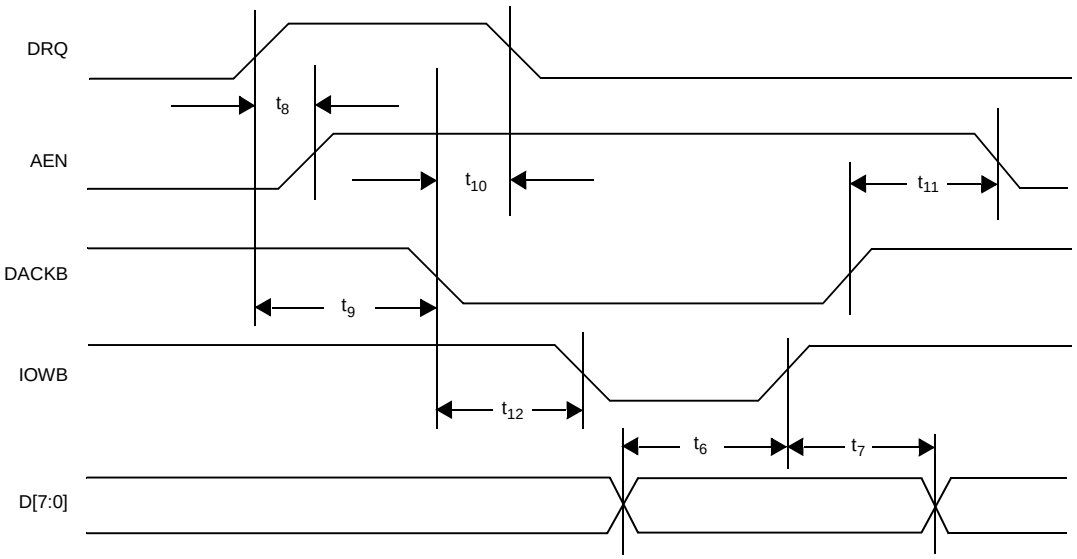


Figure 22 Compatibility Mode DMA Write Cycle

Note: In Compatibility Mode DMA, the DMA request is reset by the acknowledge going low. In Extended Mode DMA, the DMA request is reset when the acknowledge signal is low AND the correct command signal is low -- either IORB (for DMA read from I/O device) or IOWB (for DMA writer to I/O device). For Extended Mode DMA, the time t_{10} is relative to the later of: the falling edge of the acknowledge signal, or the command signal.

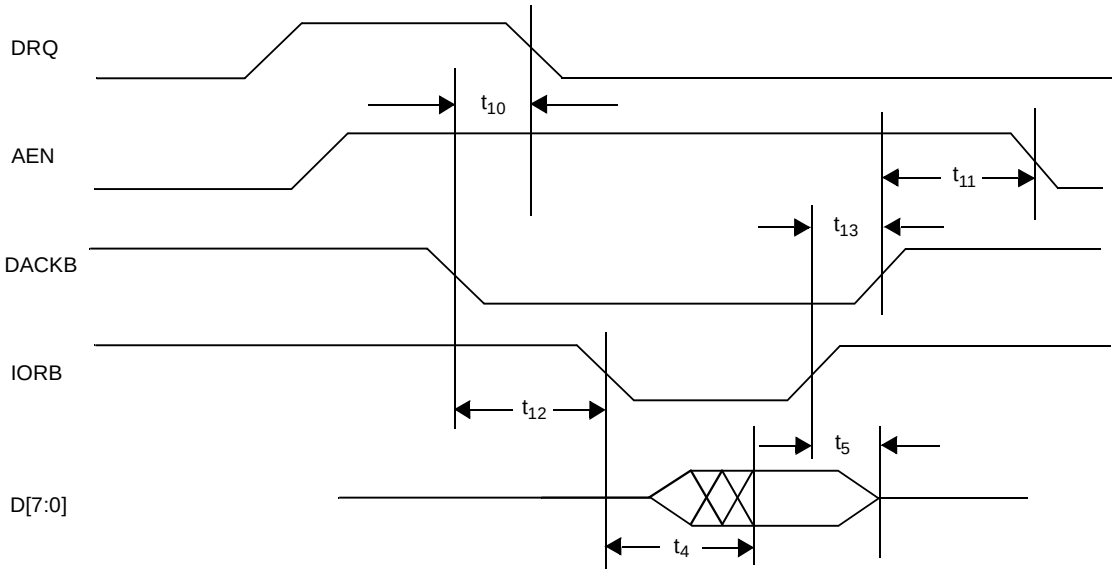


Figure 23 Compatibility Mode DMA Read Cycle

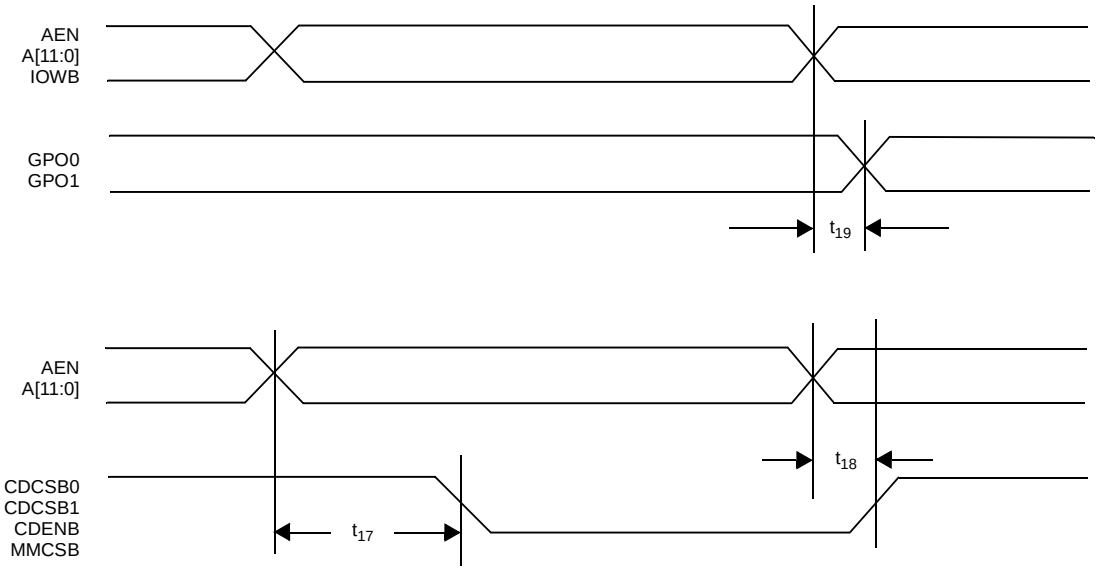


Figure 24 Miscellaneous Output Signals

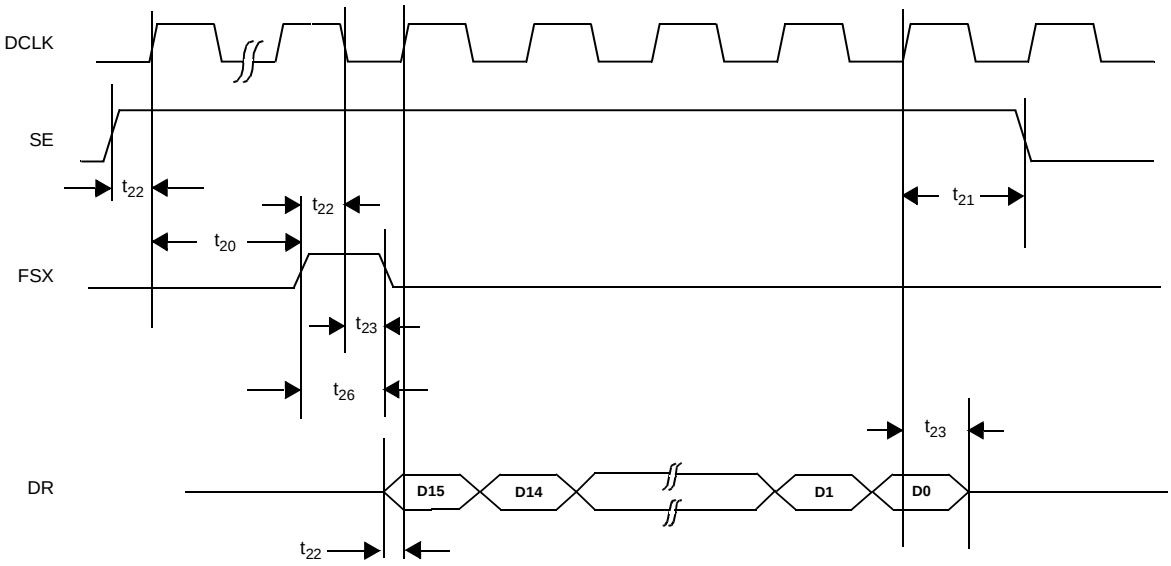


Figure 25 Serial Mode Receive Operation

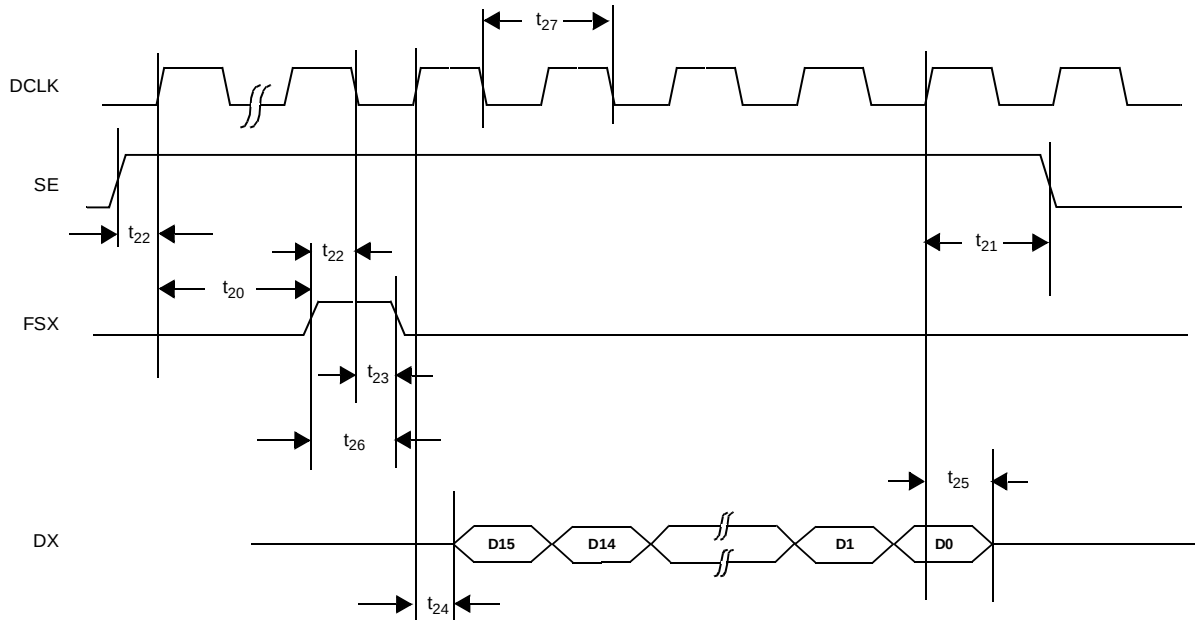


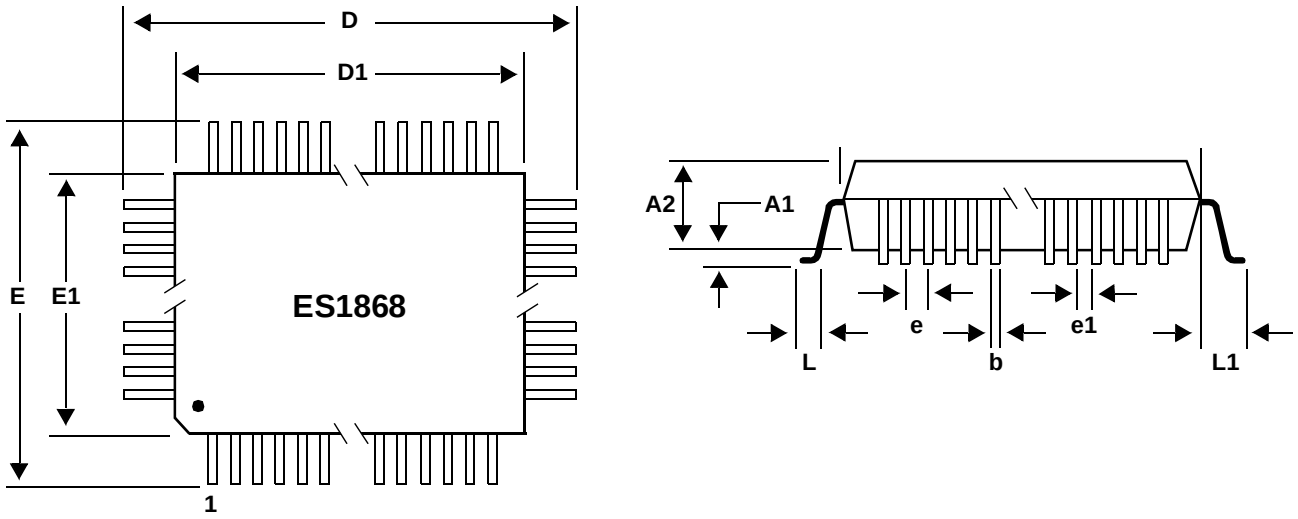
Figure 26 Serial Mode Transmit Operation

Table 19 ES1868 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_1	Reset Pulse Width	300			ns
t_2	IORB, IOWB Pulse Width	100			ns
t_3	Address Setup Time	10			ns
t_4	Read Data Access Time			70	ns
t_5	Read Data Hold Time			10	ns
t_6	Write Data Setup Time	5			ns
t_7	Write Data Hold Time	10			ns
T_8	DMA Request to AEN High	0			ns
t_9	DMA Request to DMA ACK	10			ns
t_{10}	DMA ACK to Request Release *			30	ns
t_{11}	DMA ACK High to AEN Low	0			ns
t_{12}	DMA ACK to IOWB, IORB Low	0			ns
t_{13}	IOWB, IORB to DMA ACK Release	20			ns
t_{14}	Crystal Frequency, XI/XO		14.318		MHz
t_{17}	AEN, A[11:0], CDCSB0, CDCSB1, MMCSB, CDENB Low			20	ns
t_{18}	AEN, A[11:0], CDCSB0, CDCSB1, MMCSB, CDENB High			20	ns
t_{19}	AEN, A[11:0], IOWB, IORB to GPO0, GPO1 Delays			20	ns
t_{20}	SE High to Valid FSR, FSX Edge	2			DCLK
t_{21}	SE Release Time to Last DX, DR Data Bit	1			DCLK
t_{22}	SE, FSX, FSR Setup Time to DCLK Edge	15			ns
t_{23}	SE, FSX, FSR, DR Hold Time to DCLK Edge	10			ns
t_{24}	DX Delay Time from DCLK Edge			20	ns
t_{25}	DX Hold Time from DCLK Edge	10			ns
t_{26}	FSR, FSX Pulse Width	60	500		ns
t_{27}	DCLK Clock Frequency		2.04		MHz

* Note: In Compatibility Mode DMA, the DMA request is reset by the acknowledge signal going low. In Extended Mode DMA, the DMA request is reset when the acknowledge signal is low AND the correct command signal is low – either IORB (for DMA read from I/O device) or IOWB (for DMA write to I/O device). For Extended Mode DMA, the time T_{10} is relative to the later of the falling edge of the acknowledge signal or the command signal.

MECHANICAL DIMENSIONS



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	23.65	23.90	24.15
D1	Package's outside, X-axis	19.90	20.00	20.10
E	Lead to lead, Y-axis	17.65	17.90	18.15
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.10	0.25	0.36
A2	Package thickness	2.57	2.71	2.87
b	Lead width	0.20	0.30	0.40
e	Lead pitch	-	0.65	-
e1	Lead gap	0.24	-	-
L	Foot length	0.65	0.80	0.95
L1	Lead length	1.88	1.95	2.02
-	Foot angle	0°		7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	30	-
-	Leads in Y-axis	-	20	-
-	Total Leads	-	100	-
-	Package Type	-	PQFP	-

Figure 27 ES1868 Mechanical Dimensions

APPENDIX A: ES1868 PNP ROM DATA EXAMPLE

16-bit address decode used with external device decoding. A[15:12] and AEN to be all zero.

LDN #0 Control Interface.

LDN #1 Audio (FM) MPU-401

LDN #2 Joystick

LDN #3 IDE CD-ROM

LDN #4 Modem (not used here)

Note: Contact your ESS sales representative or FAE for the most current EPROM data code for your hardware design.

```
; *******************************************************
;
; Start of ESS Proprietary Header (8 bytes)
;
; *******************************************************
0A5H; PNP OK byte
059H; IRQA = 9 IRQB = 5
0A7H; IRQC = 7 IRQD = 10
0CBH; IRQE = 11 IRQF = 12
010H; DRQA = 0  DRQB = 1
053H; DRQC = 3  DRQD = 5
002H; MPU-401 part of audio,  CD, DRQ latching off
00CH; GPO1/GPI are not used by Modem DMA channel or g.p.

; *******************************************************
;
; Start of PNP Resource Header
;
; *******************************************************
016H, 073H, 018H, 068H; "ESS1868" product id for ES1868
0FFH, 0FFH, 0FFH, 0FFH; serial number FFFFFFFF (not supported)
000H; header checksum
00AH, 010H, 010H; PNP 1.0, ESS version 1.0
082H, 023H, 000H; “ESS ES1868 Plug and Play AudioDrive”

; *******************************************************
;
; LOGICAL DEVICE 0  --  Configuration Ports
;  8 bytes at any I/O address that is a multiple of 8
;
; *******************************************************
015H, 016H, 073H, 000H, 000H, 000H; ESS0000
047H, 001H, 000H, 008H, 0F8H, 00FH, 008H, 008H; 800H-FF8H 8 bytes

; *******************************************************
;
; LOGICAL DEVICE 1 -- Audio Controller w/FM and MPU-401
;
; *******************************************************
015H, 016H, 073H, 018H, 068H, 000H; ESS1868

;  Basic configuration 0000
031H, 000H
02AH, 002H, 008H; DMA 0:   DRQ 1
02AH, 009H, 008H; DMA 1:   DRQ 0 or 3
022H, 020H, 000H; INT 0:   IRQ 5
```

```
04BH, 020H, 002H, 010H; 220-22F 16 bytes
04BH, 088H, 003H, 004H; 388-38B
04BH, 030H, 003H, 002H; 330-331

;  Basic configuration 0001
031H, 001H
02AH, 002H, 008H; DMA 0: DRQ 1
02AH, 009H, 008H; DMA 1: DRQ 0 or 3
022H, 0A0H, 006H; INT 0: IRQ 5, 7, 9, or 10
047H, 001H, 020H, 002H, 040H, 002H, 020H, 010H; 220 or 240 16 bytes
04BH, 088H, 003H, 004H; 388-38B
047H, 001H, 000H, 003H, 030H, 003H, 030H, 002H; 300 or 330 2 bytes

;  Basic configuration 0002
031H, 001H
02AH, 00BH, 008H; DMA 0: DRQ 0, 1 or 3
02AH, 00BH, 008H; DMA 1: DRQ 0, 1 or 3
022H, 0A0H, 01EH; INT 0: IRQ 5, 7, 9, 10, 11, or 12
047H, 001H, 020H, 002H, 080H, 002H, 020H, 010H; 220, 240, 260, 280 16 bytes
04BH, 088H, 003H, 004H; 388-38B
047H, 001H, 000H, 003H, 030H, 003H, 030H, 002H; 330 or 330 2 bytes

;  Basic configuration 0003
031H, 001H
002H, 00BH, 008H; DMA 0: DRQ 0, 1 or 3
02AH, 00BH, 008H; DMA 1: DRQ 0, 1 or 3
022H, 0A0H, 01EH; INT 0: IRQ 5, 7, 9, 10, 11, or 12
047H, 001H, 020H, 002H, 080H, 002H, 020H, 010H; 220, 240, 260, 280 16 bytes
04BH, 088H, 003H, 004H; 388-38B
047H, 001H, 000H, 008H, 0FEH, 00FH, 002H, 002H; 800/801-FFE/FFF 2 bytes

;  Basic configuration 0004
031H, 002H
02AH, 00BH, 008H; DMA 0: DRQ 0, 1 or 3
02AH, 00BH, 008H; DMA 1: DRQ 0, 1 or 3
022H, 0A0H, 01EH; INT 0: IRQ 5, 7, 9, 10, 11, or 12
047H, 001H, 020H, 002H, 080H, 002H, 020H, 010H; 220, 240, 260, 280 16 bytes
047H, 001H, 000H, 008H, 0FCH, 00FH, 004H, 004H; 800/804-FFC/FFF 4 bytes
047H, 001H, 000H, 008H, 0FEH, 00FH, 002H, 002H; 800/801-FFE/FFF 2 bytes

038H; end configurations

; ****************************************************
;
; LOGICAL DEVICE 2 -- Joystick
; Only choice is one address at 201.
;
; ****************************************************
015H, 016H, 073H, 000H, 001H, 000H; ESS0001

;  Basic configuration 0000
031H, 000H
04BH, 001H, 002H, 001H; 201
;  Windows95 joystick driver will only allow 200-20F!!!
;  Basic configuration 0001
031H, 001H
047H, 001H, 000H, 002H, 00FH, 002H, 001H, 001H; 200/200-20F/20F 1 byte
038H; end dependent functions
01CH, 041H, 0D0H, 0B0H, 02FH; Compatible ID: PNPB02F
```

```
; ******************************************************
;
; LOGICAL DEVICE 3 -- IDE CD-ROM
; needs an IRQ (10, 11, or 12) and two separate address ranges
;
; ******************************************************
015H, 016H, 073H, 000H, 002H, 000H; ESS0002

;  Basic configuration 0000
031H, 000H
022H, 000H, 010H; IRQ 12
04BH, 068H, 001H, 008H; 168-16F 8 bytes
04BH, 06EH, 003H, 002H; 36E-36F 2 bytes

;  Basic configuration 0001
031H, 001H
022H, 000H, 00CH; IRQ 10 or 11
04BH, 068H, 001H, 008H; 168-16F 8 bytes
04BH, 06EH, 003H, 002H; 36E-36F 2 bytes

;  Basic configuration 0002
031H, 001H
022H, 000H, 01CH; IRQ 10, 11 or 12
04BH, 0E8H, 001H, 008H; 1E8-1EF 8 bytes
04BH, 0EEH, 003H, 002H; 3EE-3EF 2 bytes

;  Basic configuration 0003
031H, 001H
022H, 000H, 01CH; IRQ 10, 11 or 12
047H, 001H, 000H, 001H, 0F8H, 001H, 008H, 008H; 100/1F8-107/1FF 8 bytes
047H, 001H, 000H, 003H, 0FEH, 003H, 002H, 002H; 300/301-3FE/3FF 2 bytes

038H; end dependent functions

01CH, 041H, 0D0H, 006H, 000H        ; Compatible ID: PNP0600
079H, 000H; end tag + checksum
```

APPENDIX B: SCHEMATIC EXAMPLES

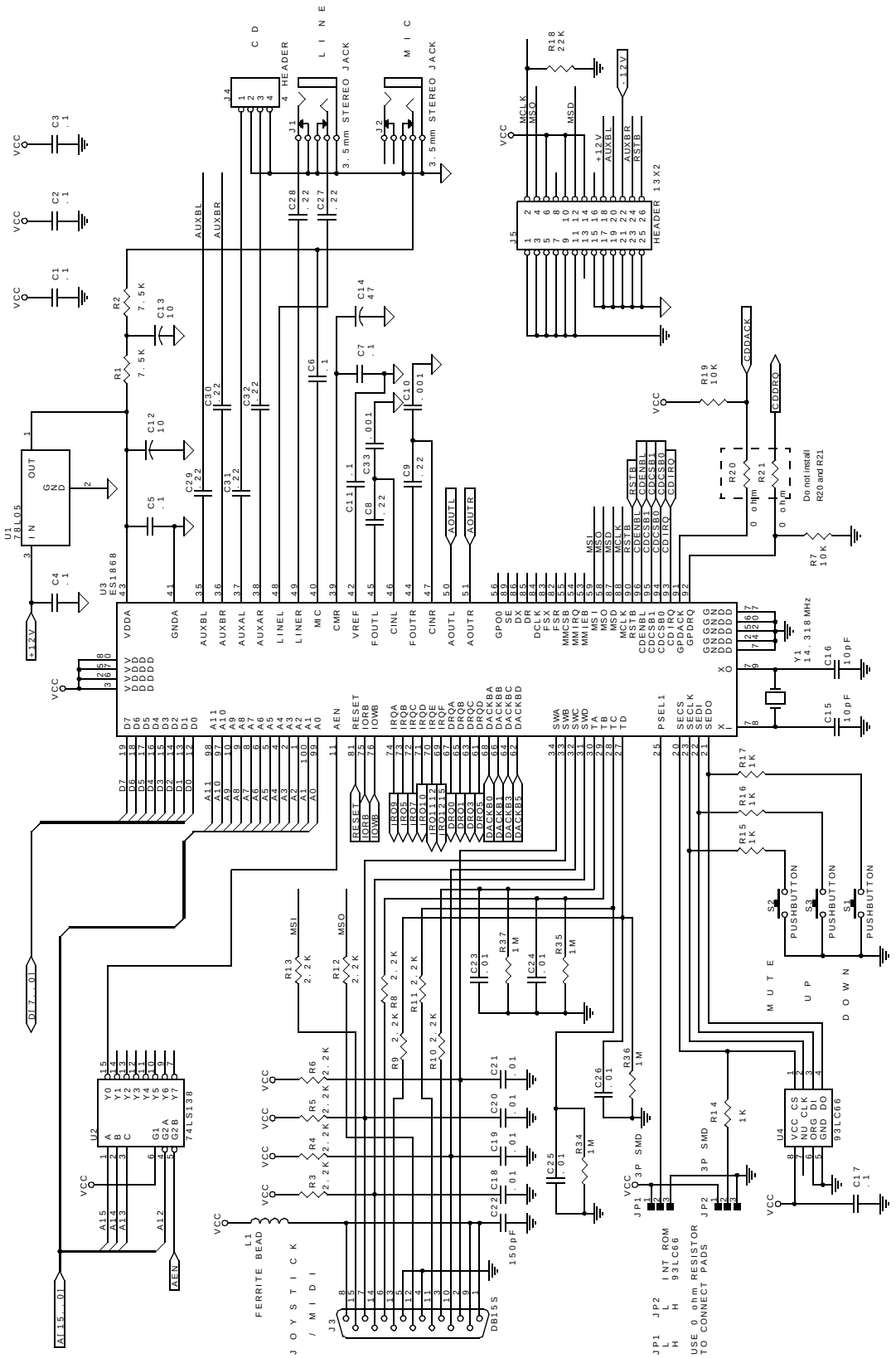


Figure 28 ES1868 Schematic

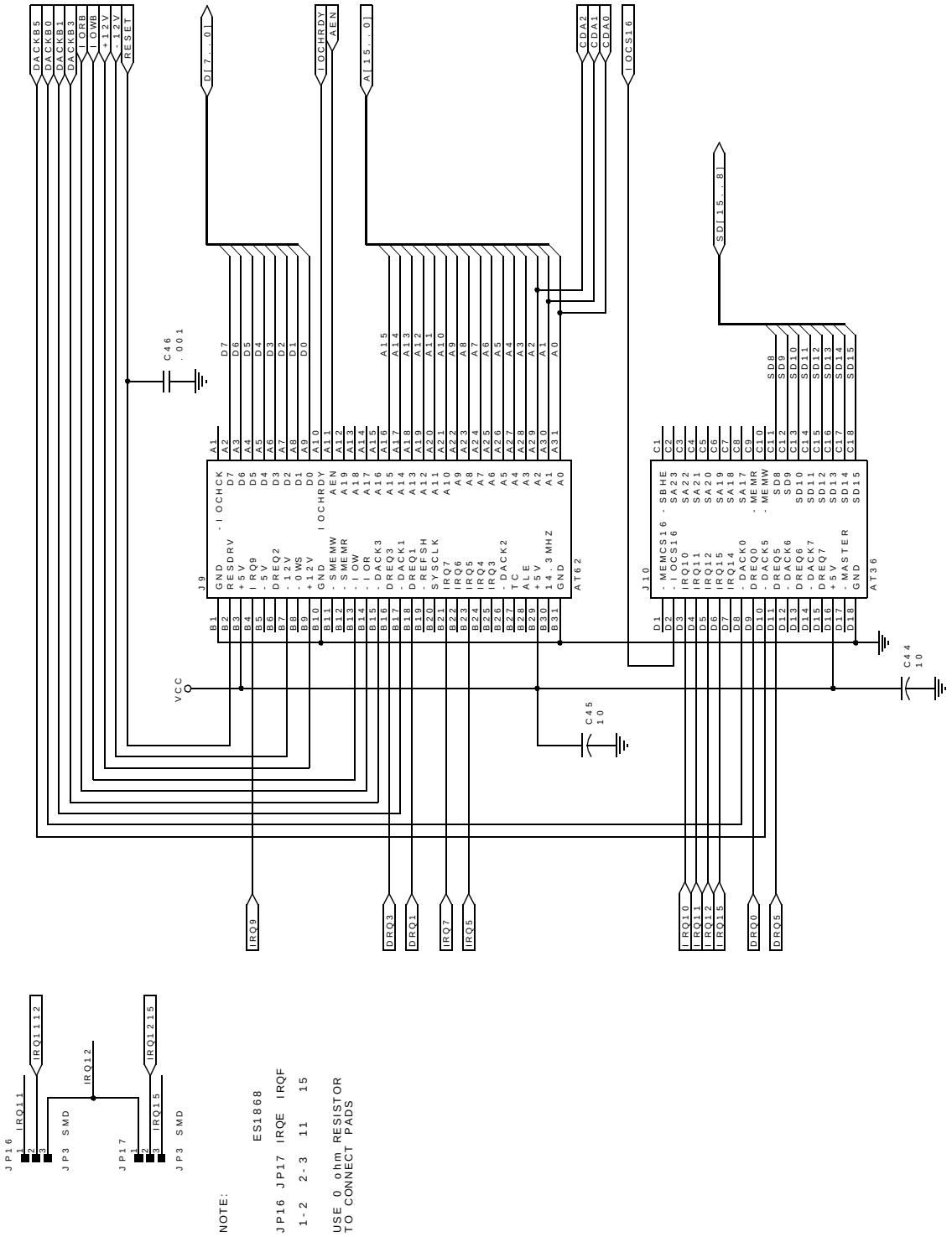


Figure 29 PC Interface

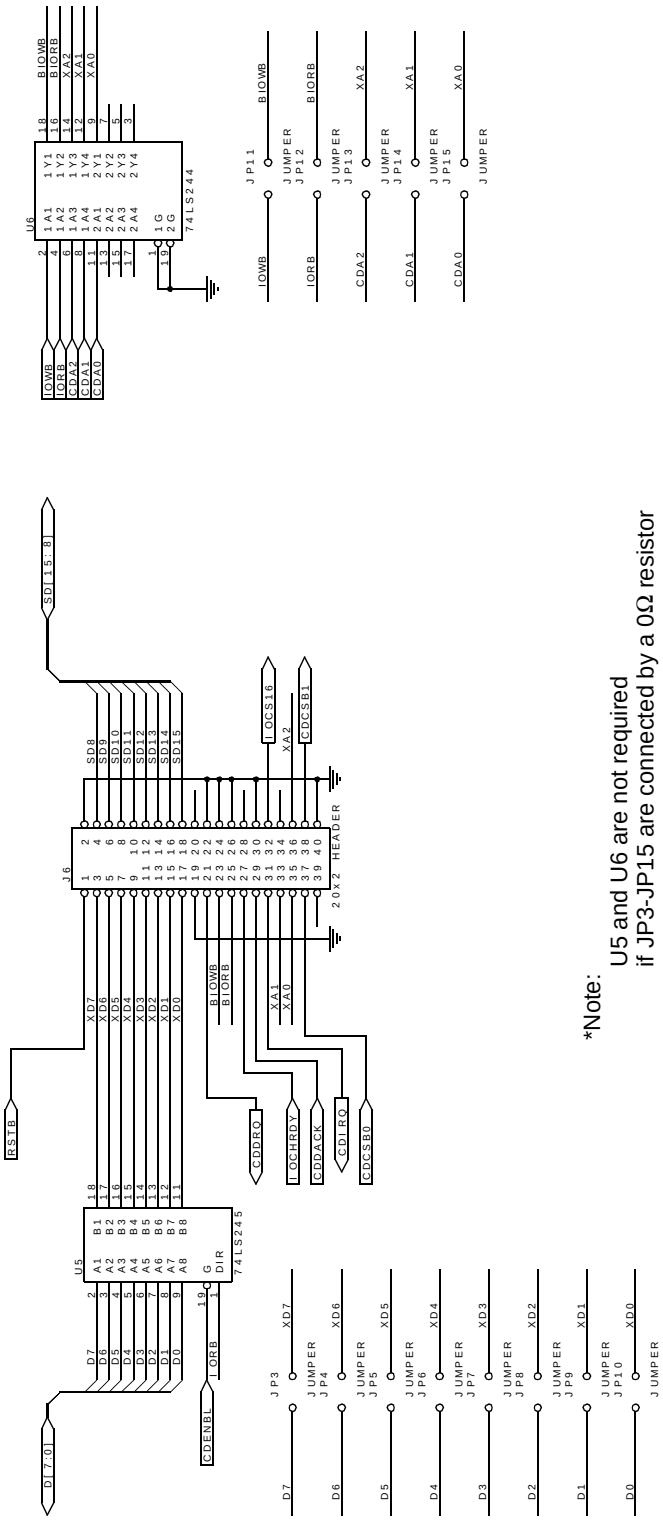


Figure 30 CD-ROM Section

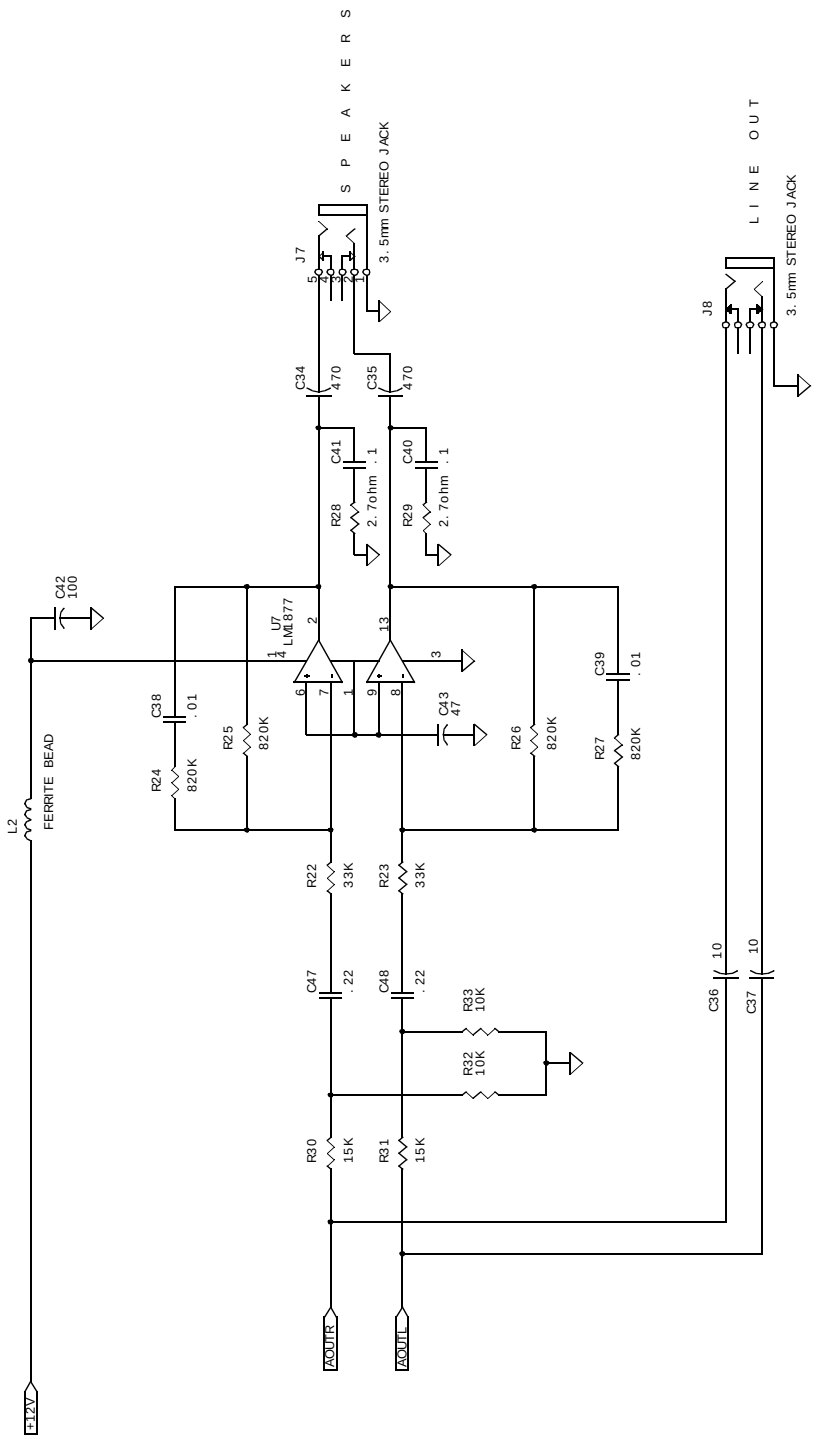


Figure 31 Amplifier Section

APPENDIX C: LAYOUT GUIDELINES

PCB Layout

Notebook, Motherboard, Pen-based, and PDA portable computers have the following similarity in PCB layout design:

1 Multi-layer (usually 4 to 8 layer).
2 Double-sided SMT.
3 CPU, corelogic (chip set), system memory, VGA controller, and video memory reside in the same PCB.

This is a very noisy environment for adding an audio circuit. The following are the guidelines for PCB layout for ESS *Audio***Drive**® chip application.

Component Placement

The audio circuit-related components must be grouped in the same area. The audio I/O jack and connector are considered audio-related components as well. There are two possible placements for these audio components:

A grouped on one side of the PCB.
B separated on both sides of the PCB.

In Case B, audio component grouping will take less space.

Analog Ground Plane

Audio circuits require two layers of analog ground planes for use as shielding for all analog traces.

In component placement case A (Figure 32), the first layer of analog ground plane is on the analog component side, the second analog ground plane is on the inner layer, and the analog traces are embedded between these two planes.

In component placement case B (Figure 33), the analog ground planes are on both sides of the PCB, with the analog traces shielded in the middle.

Case A:

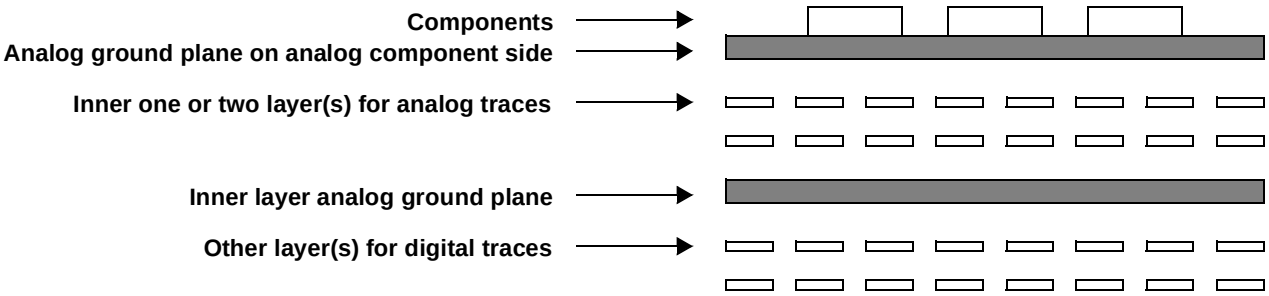


Figure 32 Analog Components on One Side of the PCB

Case B:

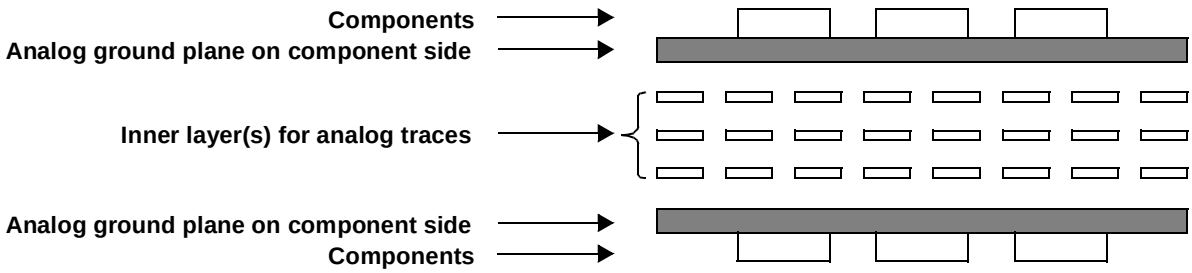


Figure 33 Analog Components on Both Sides of the PCB.

Special Notes

The analog traces should be places as short as possible.

The MIC-IN circuit is the most sensitive of the audio circuits, and requires proper and complete shielding.

APPENDIX D: ES1868 BILL OF MATERIALS

Table 20 ES1868 Bill of Materials (BOM)

Item	Quantity	Reference	Part
1	11	C1,C2,C3,C4,C5,C6,C7,C11,C17,C40,C41	.1 µF 0805
2	10	C8,C9,C27,C28,C29,C30,C31,C32,C47,C48	.22 µF 0805
3	3	C10,C33,C46	.001 µF 0805
4	6	C12,C13,C36,C37,C44,C45	10 µF Radial .100”
5	2	C14,C43	47 µF Radial .100”
6	2	C15,C16	10 pF 0805
7	10	C18,C19,C20,C21,C23,C24,C25,C26,C38,C39	.01 µF 0805
8	1	C22	150 pF 0805
9	2	C34,C35	470 µF Radial .180”
10	1	C42	100 µF Radial .100”
11	2	JP1,JP2 (Jumpered on H)	0.0 ohm resistor 0805
12	13	JP3,JP4,JP5,JP6,JP7,JP8,JP9,JP10,JP11,JP12,JP13,JP14,JP15	0.0 ohm resistor 0805
13	2	JP16 (pin1&2),JP17 (pin1&2)	0.0 ohm resistor 0805
14	4	J1,J2,J7,J8	3.5 mm STEREO JACK
15	1	J3	DB15 Female
16	1	J4 (CD-Audio)	4x1, 4-Pin HDR, 2 mm Pitch
17	1	J5 (Wavetable card)	13x2, 26-Pin HDR
18	1	J6 (CD-ROM interface)	20x2, 40-Pin HDR
19	2	L1,L2	FERRITE BEAD, SMT 0805
20	2	R1,R2	7.5K 0805
21	10	R3,R4,R5,R6,R8,R9,R10,R11,R12,R13	2.2K 0805
22	4	R7,R19,R32,R33	10K 0805
23	4	R14,R15,R16,R17	1K 0805
24	1	R18	22K 0805
25	2	R22,R23	33K 0805
26	4	R24,R25,R26,R27	820K 0805
27	2	R28,R29	2.7 ohm 0805
28	2	R30,R31	15K 0805
29	4	R34,R35,R36,R37	1M 0805
30	3	S1,S2,S3	PUSHBUTTON
31	1	U1	78L05 TO-92 SMT
32	1	U2	74LS138 SMT
33	1	U3	ES1868 PQFP-100
34	1	U4	93LC66 EEPROM SMT
35	0	U5 (Optional: use item #12, qty:8)	74LS245 SMT
36	0	U6 (Optional: use item #12, qty:5)	74LS244 SMT
37	1	U7	LM1877 SMT
38	1	Y1	14.318 MHz

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