YAMAHA LSI

YMF721

CONFIDENTIAL

OPL4-ML2

FM + Wavetable Synthesizer LSI

■ OVERVIEW

YMF721 (OPL4-ML2) is a high quality and low cost Wavetable synthesizer LSI. YMF721 (OPL4-ML2) integrates an OPL3 (FM synthesizer), General MIDI processor and 1 Mbyte Wavetable sample ROM into one chip, and complies with General MIDI (GM) system level 1. Thus, it is best suited to multimedia applications, sound cards, MIDI synthesis modules and other sound applications.

Since this LSI outputs stereophonic 16 bit digital signal (fs = 44.1 kHz), it can be connected directly with YMF701B, 711 or 715 (OPL3-SA, SA2 or SA3) or with YAC516(DAC16-L).

Operating voltage, 3.3 V, allows this LSI to be controlled with notebook personal computers.

Power management functions (power down and suspend/resume functions) of OPL4-ML2 contribute to low power consumption of personal computers into which this product is built-in.

■ FEATURES

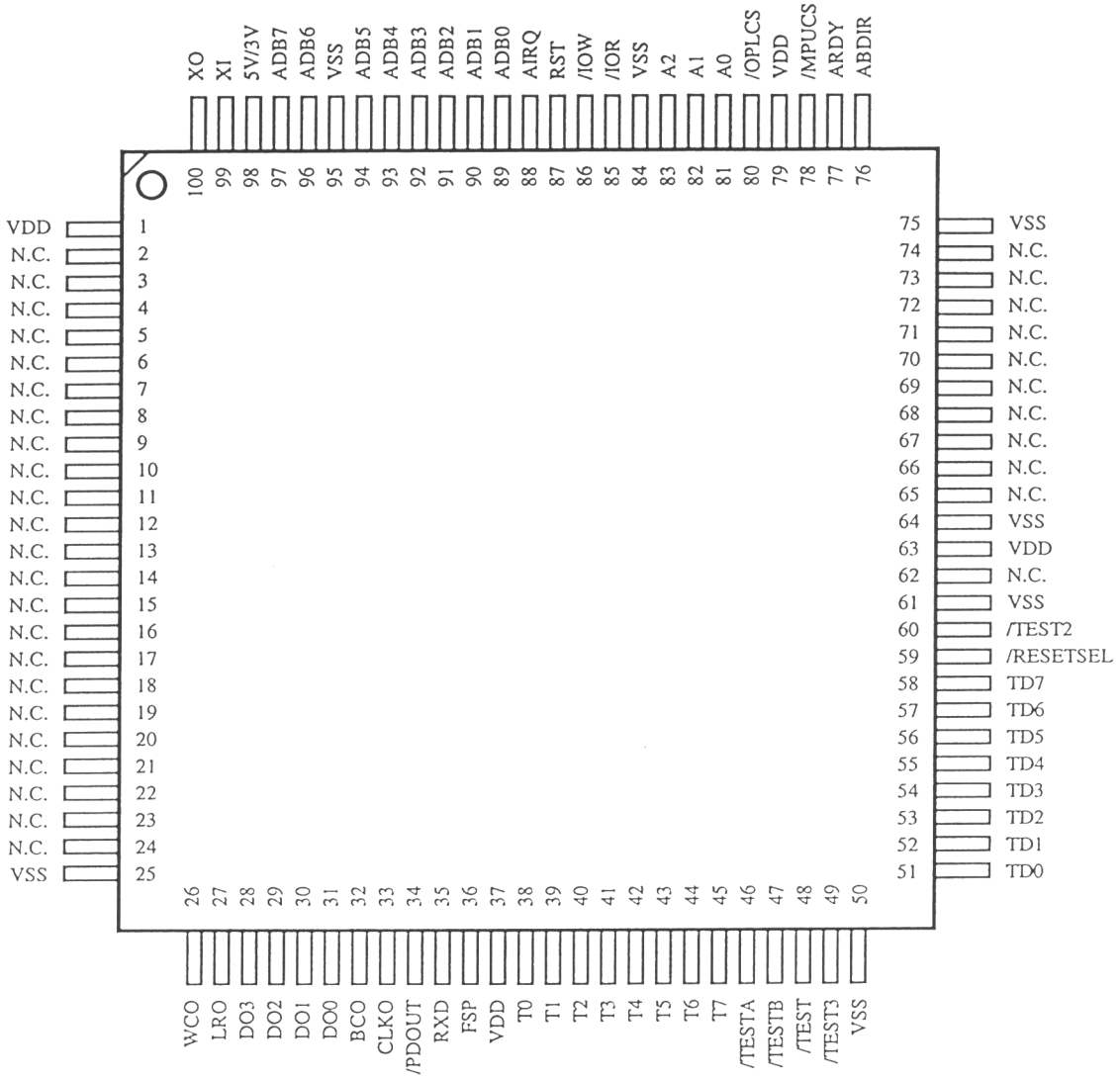
- The Wavetable synthesizer of this LSI is able to generate up to 24 types of sounds simultaneously.
- Has an interface that makes this LSI compatible with MPU-401 UART mode.
- Has an OPL3 (FM synthesizer) for AdLib/SoundBlaster applications.
- Has a 1 Mbyte built-in Wavetable sample ROM.
- Complies with GM system Level 1. (Thus, it is compatible with DOS applications that support MPU-401.)
- MIDI signal can be transmitted either through serial input or parallel input.
- FM synthesizer and Wavetable synthesizer of this LSI can generate their sound at the same time.
- FM synthesizer is register-compatible with OPL3.
- All registers are readable.
- Power management functions included power down and suspend/resume can be supported.
- Frequency of master clock signal is 33.8688 MHz.
- Pin compatible with YMF704C-S (100 pin SQPF)
- Voltage of power supply can be 5.0 V or 3.3 V.
- Silicone gate CMOS process
- 100-pin SQFP (YMF721-S).

YAMAHA CORPORATION

May 20, 1997

■ PIN CONFIGURATION

YMF721-S



100 pin SQFP Top View

■ PIN DESCRIPTION

ISA bus interface : 19 pins					
Pin name	pins	I/O	Type	Size	Function
ADB7-0	8	I/O	TTL	2mA	Data bus
A2-0	3	I	TTL	-	Address bus
/MPUCS	1	I	TTL	-	MPU401 chip select
/OPLCS	1	I	TTL	-	FM/Wavetable/Command/Control chip select
/IOW	1	I	TTL	-	Write enable
/IOR	1	I	TTL	-	Read enable
RST	1	I	TTL	-	Initial clear input
AIRQ	1	O	TTL	2mA	Interrupt signal ("H" : Interrupt)
ABDIR	1	O	TTL	2mA	Selection of data transfer direction ("L" : YMF721→Host)
ARDY	1	OD	TTL	12mA	I/O channel ready/busy selection ("L" : Busy)

MIDI interface : 2 pins					
Pin name	pins	I/O	Type	Size	Function
RXD	1	I	TTL	-	MIDI serial data input
FSP	1	I	TTL	-	Selection of MIDI serial/parallel transmission ("H" : Parallel, "L" : Serial)

Serial audio interface : 8 pins					
Pin name	pins	I/O	Type	Size	Function
CLKO	1	O	CMOS	8mA	Clock output (384fs = 16.9344MHz)
BCO	1	O	CMOS	2mA	Bit clock output (48fs = 2.1168MHz)
LRO	1	O	CMOS	2mA	L/R clock output (fs = 44.1kHz)
WCO	1	O	CMOS	2mA	Word clock output (2fs = 88.2kHz)
DO3	1	O	CMOS	2mA	Effect send output
DO2	1	O	CMOS	2mA	MIX (FM + Wavetable) output
DO1	1	O	CMOS	2mA	Wavetable output
DO0	1	O	CMOS	2mA	FM output

Others : 39 pins					
Pin name	pins	I/O	Type	Size	Function
5V/3V	1	I	CMOS	-	Selection of power supply
/RESETSEL	1	I+	TTL	-	RST signal polarity control pin (When this pin is at "L", RST is active at "L".)
/PDOUT	1	O	CMOS	2mA	Power down control output
XI	1	I	CMOS	2mA	Crystal oscillator connection or master clock input (33.8688 MHz)
XO	1	O	CMOS	2mA	Crystal oscillator connection pin
N.C.	34	-	-	-	To be open at normal use.

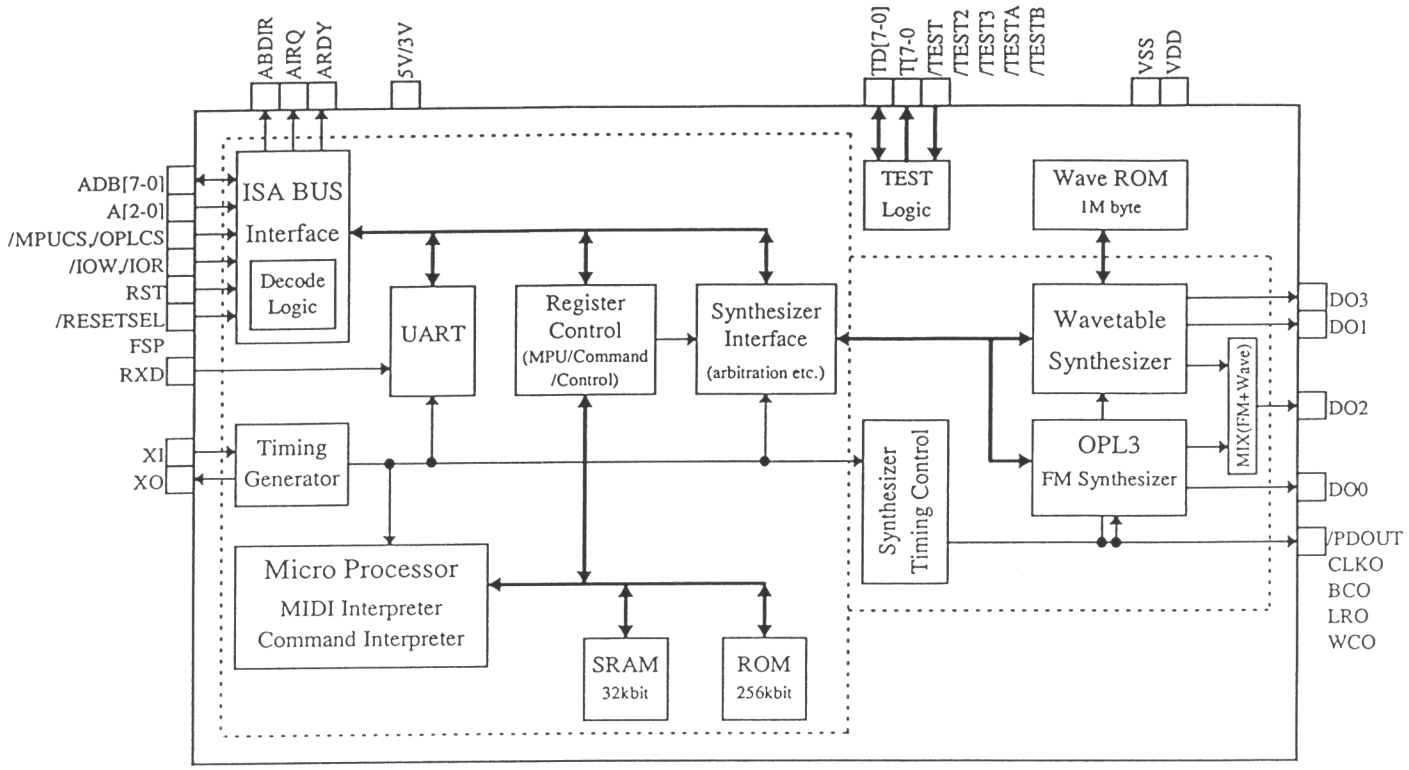
LSI test pins : 21 pins					
Pin name	pins	I/O	Type	Size	Function
/TESTA	1	I+	TTL	-	To be open at normal use.
/TESTB	1	I+	TTL	-	To be open at normal use.
/TEST	1	I+	TTL	-	To be open at normal use.
/TEST2	1	I+	TTL	-	To be open at normal use.
/TEST3	1	I+	TTL	-	To be open at normal use.
T7-0	8	O	CMOS	2mA	To be open at normal use.
TD7-0	8	I/O	CMOS	2mA	To be open at normal use.

Power supply, ground : 11 pins					
Pin name	pins	I/O	Type	Size	Function
VDD	4	-	-	-	Power supply (put on +5.0 V or +3.3V)
VSS	7	-	-	-	Ground

Total : 100 pins

Note : I+ : Input pin with built-in pull-up resistor, OD : Open drain output pin

■ BLOCK DIAGRAM



■ FUNCTIONS

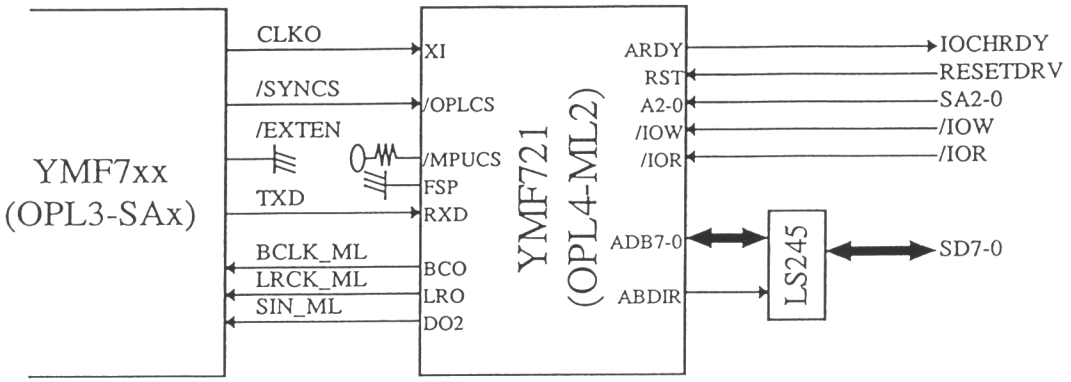
1. 1. Example of system configuration

1-1. System with MPU401 UART

This section describes two examples of systems that have an MPU401 UART in them.

In these examples, YMF701B, 711 or 715 (OPL3-SA, SA2 or SA3) has a built-in MPU401 UART.

(1) ISA BUS Connect System



Note :

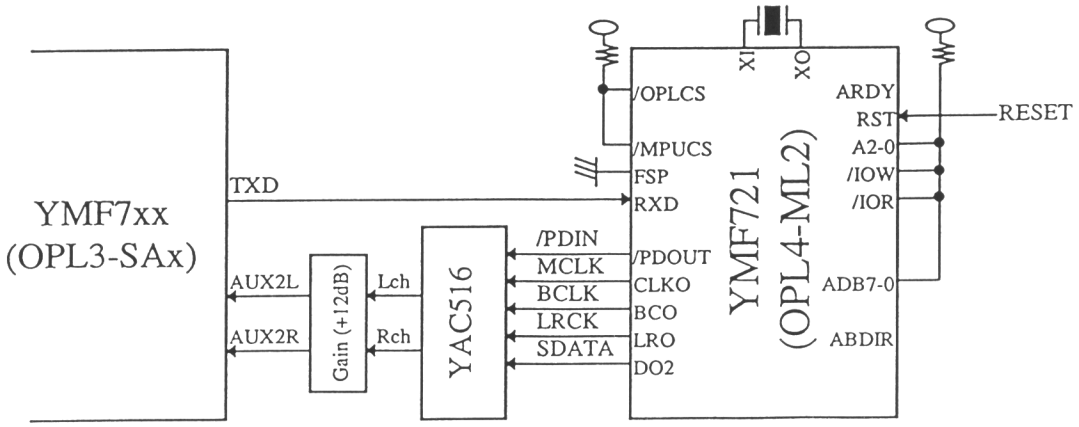
YMF721 (OPL4-ML2) has MPU401 UART in it. Thus, for the above case, TXD of YMF7xx (OPL3-SAx) is connected with RXD of YMF721 (OPL4-ML2) and MPU401 port (/MPUCS) of YMF721 (OPL4-ML2) is disabled so that YMF7xx(OPL3-SAx) sends MIDI data directly to YMF721 (OPL4-ML2).

For the above case, FM synthesizer of YMF7xx (OPL3-SAx) is disabled and the one in YMF721 (OPL4-ML2) is made active. (This control is made through /EXTEN pin of YMF7xx.) For the above system, the data bus that connects with YMF721(OPL4-ML2) gains access to FM-synthesizer/Command/Control port of YMF721(OPL4-ML2). (Chip select signal is outputted from /SYNCS pin of YMF7xx.)

For the source of master clock to be inputted to XI pin of YMF721 (OPL4-ML2), it is recommended to use CLKO pin of YMF7xx (OPL3-SAx). For other methods, a crystal oscillator can be used by attaching it to XI and XO pins of YMF721 (OPL4-ML), or a clock of 33.8688 MHz supplied from the system can be used.

When serial data outputs of YMF721 (OPL4-ML2), BCO, LRO and DO2 pins, are connected with external serial data interface (BCLK_ML, LRCK_ML, SIN_ML) of YMF7xx (OPL3-SAx), the serial data is converted to analog signal in YMF7xx (OPL3-SAx) and outputted as analog signal.

(2) No ISA BUS Connect System



Note :

YMF721 (OPL4-ML2) has MPU401 UART in it. Thus, for the above case, TXD of YMF7xx (OPL3-SAx) is connected with RXD of YMF721 (OPL4-ML2) and MPU401 port (/MPUCS) of YMF721 (OPL4-ML2) is disabled so that YMF7xx(OPL3-SAx) sends MIDI data directly to YMF721 (OPL4-ML2).

The above system does not connect YMF721 (OPL4-ML2) and ISA bus, which is an example of Wavetable upgrade solution represented by the Wavetable daughter card. Input pins of the ISA bus interface should be pulled up externally. At this time, FM synthesizer/Command/Control ports are disabled, but the power down function is enabled by receiving System Exclusive Message on the MIDI data, except that Suspend/Resume function is disabled.

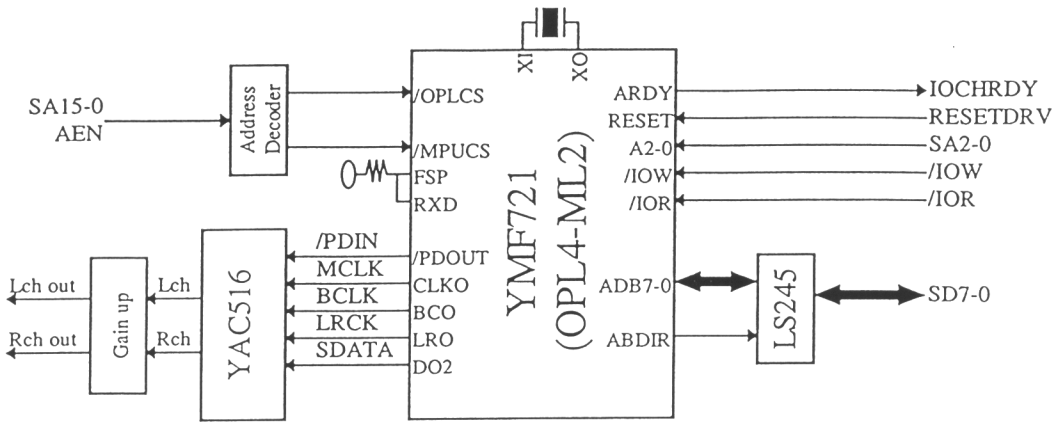
As a source of master clock for YMF721 (OPL4-ML2), use a crystal oscillator by connecting it to XI and XO pins, or use the clock of 33.8688 MHz from the system. Connect BCO, LRO, DO2, /PDOUT and CLKO directly to YAC516 (DAC16-L) as shown to convert serial data output to analog signal. Then, it is recommended to input the converted analog signal to AUX2L and AUX2R of YMF7xx (OPL3-SAx) after amplifying the volume of source of YMF721 through the gain of +12 dB as shown for the purpose of equalizing the volumes of multiple sources.

1-2. System without MPU401 UART

This section describes an example of a system that does not have MPU401 UART in it.

In this example, MPU401 UART of YMF721 (OPL4-ML2) is used.

FM synthesizer of this LSI is compatible with applications that support AdLib/Sound Blaster, and Wavetable synthesizer is compatible with applications that support MPU401.



Note :

For the above case, MPU401 port of YMF721 (OPL4-ML2) must be made active because the system does not have MPU401 UART in it. Addresses of standard ports through which reading or writing of registers of YMF721 (OPL4-ML2) is made are as follows.

1) /OPLCS : 388 - 38Fh (8byte)

2) /MPUCS : 330 - 331h (2byte)

As a source of master clock for YMF721 (OPL4-ML2), use a crystal oscillator by connecting it to XI and XO pins, or use the clock of 33.8688 MHz from the system. Connect BCO, LRO, DO2, /PDOUT and CLKO directly to YAC516 (DAC16-L) as shown to convert serial data output to analog signal. Then, it is recommended to amplify the volume of source of YMF721 through the suitable gain as shown for the purpose of equalizing the volumes of multiple sources.

2. ISA bus interface

8 bit parallel I/O of YMF721 (OPL4-ML2) can be connected with ISA bus. The ISA bus interface allows transfer of commands between the each block of YMF721 (OPL4-ML2) and host.

Data Bus & Address Bus

ADB7-0	: ISA data bus
A2-0	: ISA address bus
/MPUCS	: MPU401 chip select
/OPLCS	: FM/Wavetable/Command/Control chip select
/IOW	: ISA write enable
/IOR	: ISA read enable
ABDIR	: Data bus direction switching ("L" : YMF721 → ISA)
ARDY	: I/O channel ready ("L" : busy)

Control of the data bus is made with /MPUCS, /OPLCS, /IOW and /IOR signals. The mode of control of the data bus varies as follows according to the combination of states of the signals. The direction of data transfer on the data bus is determined by ABDIR. In normal operation, the internal data bus of YMF721 (OPL4-ML2) connects the built-in processor and FM/Wavetable synthesizer blocks. Every time the ISA bus accesses the register for FM/Wavetable, an internal arbitration circuit causes the internal bus to connect ISA bus and FM/Wavetable synthesizer blocks. YMF721 (OPL4-ML2) uses I/O channel ready (ARDY pin) as the internal arbitration circuit. ARDY becomes "L" (busy) every time data bus accesses the register for FM/Wavetable.

/MPUCS	/OPLCS	/IOW	/IOR	A2	A1	A0	MODE
L	H	H	L	×	L	L	MPU401 Acknowledge (FEh)
L	H	L	H	×	L	L	MPU401 MIDI Data write
L	H	H	L	×	L	H	MPU401 Status read
L	H	L	H	×	L	H	MPU401 Command write
H	L	H	L	L	L	L	FM-synth. Status read
H	L	L	H	L	H/L	L	FM-synth. Address write
H	L	L	H	L	×	H	FM-synth. Data write
H	L	H	L	L	×	H	FM-synth. Data read
H	L	H	L	H	L	L	Wavetable-synth. Status read
H	L	L	H	H	L	L	Wavetable-synth. Address write
H	L	L	H	H	L	H	Wavetable-synth. Data write
H	L	H	L	H	L	H	Wavetable-synth. Data read
H	L	H	L	H	H	L	Command response read
H	L	L	H	H	H	L	Command write
H	L	L	H	H	H	H	Control write
H	L	H	L	H	H	H	Status read
H	L	H	H	×	×	×	No-active or UART mode
H	H	×	×	×	×	×	No-active or UART mode

Notes:

× : Don't care

When address has been written into FM block, the time required to wait until writing of address or data into Wavetable block is started is 0 (zero) nsec. When address has been written into Wavetable block, the time required to wait until writing of address or data into FM block is started is also 0 (zero) nsec. When FM block has been accessed, it is necessary to wait 860 nsec or more before the FM block can be accessed again.

Interrupt

AIRQ : Interrupt signal ("H" : Interrupt)

YMF721 (OPL4-ML2) is able to provide one interrupt signal. There are two types of sources of this interrupt signal as follows.

1) Two timer flags that are used for tempo counter of FM synthesizer

2) The flag that occurs when internal processor writes data into the Command response register

The flags described in 2) is disabled as a default.

3. Serial audio interface

YMF721 (OPL4-ML2) can be connected directly with an external DAC such as YAC516 through BCO, LRO, WCO and DO3-0 pins.

BCO... Outputs bit clock. The frequency of this clock is 48 fs. (fs is the sampling frequency that is equal to the frequency of clock outputted from LRO.) Typical duty factor of this signal is 50 %.

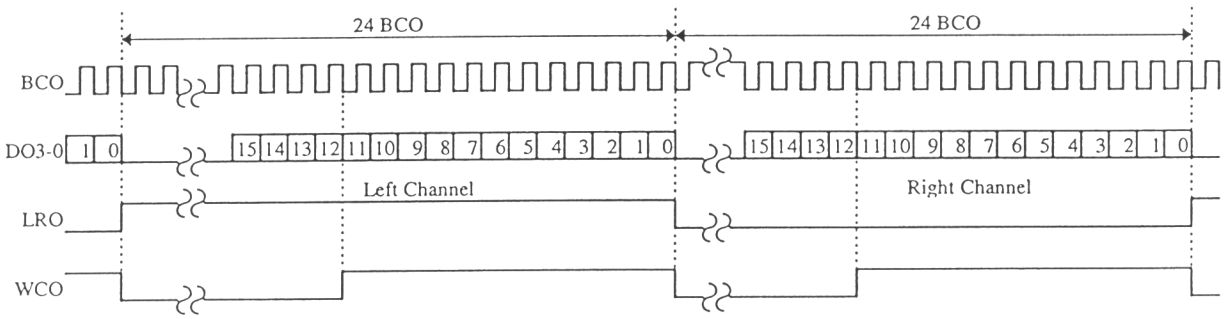
LRO... Specifies a channel for serial audio data. When LRO is "H", data is outputted from left channel, or when "L", from right channel. Frequency of this clock is 44.1 kHz. Typical duty factor of this signal is 50 %.

WCO... Frequency of this clock is 88.2 kHz. Typical duty factor of this signal is 50 %.

DO3-0... These pins output serial audio data as follows.

- DO3... Outputs data of Wavetable whose effect send level has been adjusted.
- DO2... Outputs data that is the mixture of those of FM and Wavetable.
- DO1... Outputs Wavetable data.
- DO0... Outputs FM data.

Format of the serial audio interface is as follows.



Format of YMF721 (OPL4-ML2) serial audio interface

4. MIDI Interface

MIDI serial data can be inputted from RXD pin. It is necessary to input MIDI data complied with MIDI 1.0 detailed specification to RXD pin.

The serial data is the rate of 31.25kbit/sec (+/-1%) and the unit of 10 bits. The first bit is a start bit, the next 8 bits are data (LSB to MSB), and the 10th bit is a stop bit.

5. Power management functions

YMF721 (OPL4-ML2) has two types of power management functions as follows.

(1) Global power down mode

(2) Suspend/Resume mode

5-1. Global power down mode

Generation of clock signal is disabled (stopped). Total power consumption of YMF721 (OPL4-ML2) is approximately 20uA (typ.). Writing "FDh" into command register or receiving System Exclusive MIDI Message makes in this mode. YMF721 (OPL4-ML2) outputs "L" from /PDOUT pin in this mode, which can be used as power down control signal for peripheral equipment. Set KON bit (FM synthesizer register) to "0" for all channels before going into this mode. Check that play back of MIDI data is stopped.

/RESETSEL pin has a built-in pull up resistor. When this pin is at "L" in this mode, the power consumption is higher by approximately 30uA than the one when this pin is open or at "H".

5-1-1. ISA BUS Connect System

When "FDh" has been written into command register, the internal processor goes into the global power down mode after performing the following internal processes.

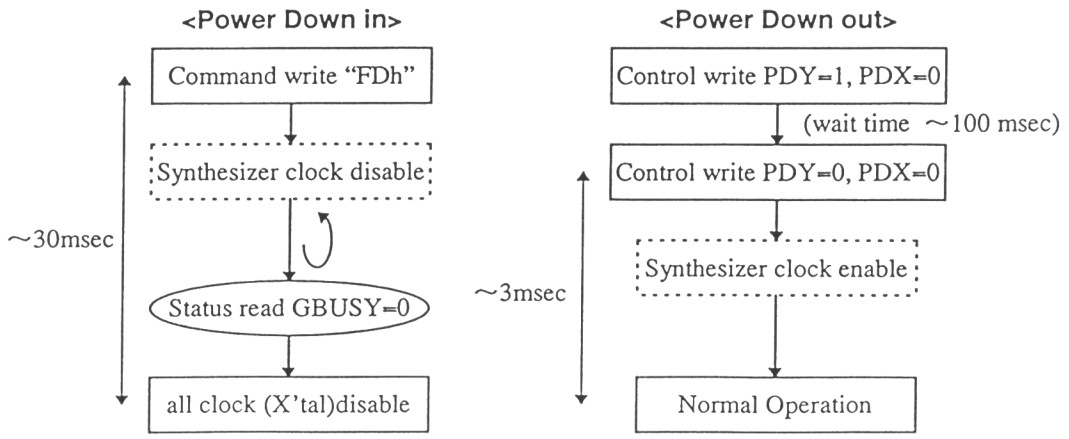
1) Disabling synthesizer's internal clock

2) Setting GBUSY bit of status register to "0".

YMF721 (OPL4-ML2) requires over 30 msec to complete the above processes before going into the power down mode.

Since generation of the clock has been disabled, recovery from the power down mode can not be made by using command. Thus, it is necessary to use PDY and PDX bits of control register for the recovery. To resume normal operation through the recovery sequence, waiting time of 50 to 100 msec is required before the oscillation of crystal stabilizes when internal oscillation is used, or 3 msec or more before the recovery of clock generated in the synthesizer.

For the details of power down command, refer to 6-3. After the power down command, FDh, has been written, do not write any command before sending a recovery command to the control register to return to the normal mode.



Power down sequence when connected with ISA bus

5-1-2. No ISA BUS Connect System

When YMF721 (OPL4-ML2) is not connected with ISA bus, power down operation can be controlled by sending Yamaha's original System Exclusive Message as the MIDI data. The System Exclusive Message includes the following three byte ID.

43h, 79h, 04h : Yamaha YMF721(OPL4-ML2) ID

The System Exclusive Message is as follows.

F0h, <Yamaha YMF721(OPL4-ML2) ID>, <Command>, <Data>, F7h

YMF721 (OPL4-ML2) supports the following commands and data.

Command	Data	Function
0Eh	6Dh	Power Down Command
0Fh	6Bh	Internal Micro-processor Reset Command

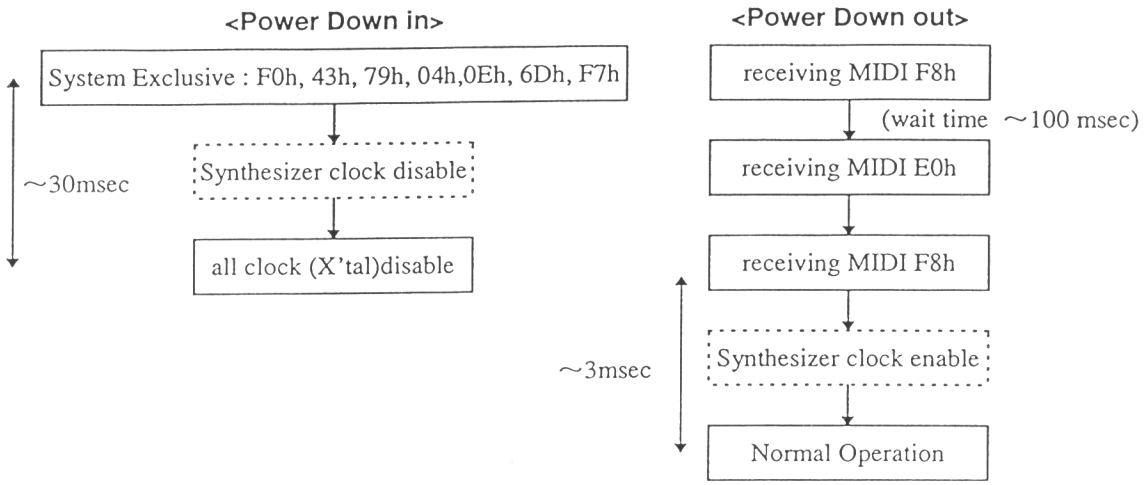
<Power Down Sequence>

(1) Power Down in

When YMF721 (OPL4-ML2) has received the System Exclusive Message shown above, it goes into the global power down mode after performing the processes as described in "5-1-1. ISA BUS Connect System".

(2) Power Down out

Since the clock generation has been disabled, YMF721 (OPL4-ML2) is not able to recover from the global power down mode by using the System Exclusive Message. Thus, the LSI needs to receive the "3byte MIDI data" as shown below to recover from the global power down mode. To resume normal operation through the recovery sequence, waiting time of 50 to 100 msec is required before the oscillation of crystal stabilizes when internal oscillation is used, or 3 msec or more before the recovery of clock generated in the synthesizer.



Power down sequence without ISA bus

<Micro-processor Reset>

The internal microprocessor is reset by receiving the above System Exchange Message.

5-2. Suspend/Resume mode

The state of internal processor is suspended by writing "E0h" into the command register before turning off the power. When the power has been turned on, it can be resumed by resetting it, writing "E1h" into the command register and then writing data that has been read before suspended.

On FM synthesizer block, check setting KON bit to "0" for all channels before reading out all register and turning off the power. Write register that has been read after turning on and resetting at the recovery sequence.

For the details of suspend/resume, refer to 6-3.

Note :

The system that includes YMF721 not connected with ISA bus can not support the suspend/resume function.

6. Registers

6-1. MPU401 compatible register

MPU401 is a generally used interface for controlling MIDI devices on the personal computer. I/O addresses that are compatible with MPU401 are as follows.

MPU_Base+ 0	(W/R)	MIDI Data transmit/acknowledge port
MPU_Base + 1	(R)	Status Register port
MPU_Base + 1	(W)	Command Register port

MIDI Data Write Port (WO):

port	D7	D6	D5	D4	D3	D2	D1	D0
MPU_Base + 0	MIDI Data							

MIDI Data... Port for writing MIDI data (transmitting). Transmission of the data must be carried out while the transmitter of MIDI data is watching the state of DRR bit of the status register. An interrupt occurs in the internal processor when MIDI data has been written into the register. Since YMF721 (OPL4-ML2) has no output signal for transmitting MIDI data, the MIDI data written into this register is used to operate internal Wavetable synthesizer.

MPU Acknowledge Port (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
MPU_Base + 0	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"0"

Sends acknowledge for the operation of MPU401.

When operation of the MPU401 is normal, "FEh" is read from this port.

Status Register Port (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
MPU_Base + 1	DSR	DRR	"1"	"1"	"1"	"1"	"1"	"1"

DSR... This bit is "1" when reading the acknowledge from MPU401. This bit is "0" when writing commands.

DRR... This bit is "1" while MIDI data is being written into MPU Data Write port (MPU Base+0). This bit is "0" when the MIDI data can be written into the MPU Data Write port. Do not write MIDI data when this bit is "1".

Default : BFh

Command Register Port (WO):

port	D7	D6	D5	D4	D3	D2	D1	D0
MPU_Base + 1	COMMAND Data							

COMMAND Data... The data written into this register is ignored. DSR bit is set to "0" when data is written into this register.

6-2. Command/Response register

I/O port for power down and suspend/resume register is described here.

Command/Response Port (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
OPL_Base + 6	Command Write							
OPL_Base + 6	Response Read							

Command Write... An interrupt occurs when data has been written into this register.

Response Read... Response to a command is read from this register.

Note :

For the details of Command/Response, refer to 6-3.

6-3. Details of command register

Some of commands supported in the command register are as follows.

Command	Sub Command	Command Length	Response Length	Function
E0h	-	1 byte	variable	Reading suspend information
E1h	00h	variable	-	Resume
FDh	-	1 byte	-	Moving into power down mode
FEh	-	1 byte	-	Checking operating conditions
FFh	-	1 byte	-	Discontinuing command execution

6-3-1. Suspend information

Command and response have the following formats.

Command		Response	
E0h	Command byte	FFh	Response 1st byte
		length L	data length (lower 8bit)
		length H	data length (upper 8bit)
		data_0	data
		.....	.....
		data_n	last data
		checksum	checksum (8 bit)

Checksum is determined so that lower eight bits of the sum of values from length L to checksum becomes "0".

The state of internal processor immediately before execution of this command can be resumed by writing the data that is read into the internal processor by using resume command described below.

6-3-2. Resume

Command and Response have the following formats.

Command		Response
E1h	Command byte	None
0x00	Sub Command	
data_0	data	
.....	.....	
data_n	last data	
checksum	checksum	

For Resume, data following the sub command are transmitted as seven bit data. Thus, it is necessary to send the data obtained with suspend command to the internal processor after encoding it. Checksum is determined so that the result of logical product (AND) of 7Fh and the sum of sub command byte, encoded data and checksum becomes "0". The internal processor returns to the state immediately before execution of Command E0h when it confirms that the data has been received normally.

6-3-3. Others

YMF721(OPL4-ML2) can use the following special commands that do not send response.

1) Command FDh : Power down mode

Refer to 5-1.

When the power down command FDh has been written into the command register, do not write any command before the return command to the control register has been executed.

2) Command FEh : Checking operating state of internal processor

This command is used to check if the internal processor is operating normally.

The internal processor is deemed operating normally if GBUSY bit of Status register is "0".

3) Command FFh : Discontinuing command execution

This command is used to discontinue the execution of a command. This command can be used only when another command is being executed.

6-4. Control/Status register

I/O port for Control/Status register is described here.

Control/Status Port (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
OPL_Base + 7(W)	PDY	PDX	-	-	-	MPR	"0"	"1"
OPL_Base + 7(R)	PDY	PDX	-	BSEL	-	RESP	GBUSY	GDRQ

PDY, PDX... YMF721 recovers from power down mode by using the following sequence.

PDY="1", PDX="0"

↓ wait time (in case of using crystal oscillation)

PDY="0", PDX="0"

D7 and D6 bits of Status register become "1" during power down mode. In this state, oscillation of clock can be confirmed by monitoring the status bit during power down mode in/out sequence.

MPR... Setting this bit to "0" initializes internal processor. Default value of this bit is "1".

BSEL... This bit shows connection of internal bus of YMF721(OPL4-ML2). Default value of this bit is "1".

"1" : Connecting synthesizer and internal processor

"0" : Connecting synthesizer and ISA bus

RESP... Indicates that a response to a command has been received.

GBUSY... Flag bit that indicates if data can be written into Command write register.

"1" : BUSY

"0" : Data can be written

GDRQ... Flag bit that indicates if data can be read from Response register.

"1" : READY

"0" : Reading is inhibited

Default : $(00x1\ x000)_{b0}$

6-5. FM synthesizer registers

6-5-1. Status register

Status Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
OPL_Base + 0	IRQ	FT1	FT2	-	-	-	LD	BUSY0

Note :

Since NEW2 (index 05h of Register array1) = 1 in default state, both LD and BUSY0 bits are valid. (LD and BUSY0 bits are invalid when NEW2=0.) BUSY0 is a BUSY flag for both FM and Wavetable registers.

6-5-2. Data register

Data Register Array 0 (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
00 - 01h	LSI TEST							
02h	TIMER 1							
03h	TIMER 2							
04h	RST	MT1	MT2	-	-	-	ST2	ST1
08h	-	NTS	-	-	-	-	-	-
20 - 35h	AM	VIB	EGT	KSR	MULT			
40 - 55h	KSL		TL					
60 - 75h	AR				DR			
80 - 95h	SL				RR			
A0 - A8h	F-NUM (L)							
B0 - B8h	-	-	KON	BLOCK			F-NUM (H)	
BDh	DAM	DVB	RHY	BD	SD	TOM	TC	HH
C0 - C8h	CHD	CHC	CHB	CHA	FB			CNT
E0 - F5h	-	-	-	-	-	WS		

Data Register Array 1 (R/W)

Index	D7	D6	D5	D4	D3	D2	D1	D0
00 - 01h	LSI TEST							
04h	-	-	CONNECTION SEL					
05h	-	-	-	-	-	NEW3	NEW2	NEW
20 - 35h	AM	VIB	EGT	KSR	MULT			
40 - 55h	KSL		TL					
60 - 75h	AR				DR			
80 - 95h	SL				RR			
A0 - A8h	F-NUM (L)							
B0 - B8h	-	-	KON	BLOCK			F-NUM (H)	
C0 - C8h	CHD	CHC	CHB	CHA	FB			CNT
E0 - F5h	-	-	-	-	-	WS		

Default :

After initial clear, all the bits of Register Array 1 are cleared to "0" except NEW2 and NEW3 bits of index 05h, and CHA and CHB bits of index C0-C8h.

For the details of these registers, refer to data sheet for YMF289B(OPL3-L).

Note :

Since NEW2 and 3 (at index 05h of Register array1) = 1 in default state, both LD and BUSY0 bits are valid. (LD and BUSY0 bits are invalid when NEW2=0.) BUSY0 is a BUSY flag for both FM and Wavetable registers.

6-6. Wavetable synthesizer register

6-6-1. Status register

Status Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
OPL_Base + 4	-	-	-	-	-	-	LD	BUSY1

6-6-2. Data register

Data Register (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
00 - 01h	LSI TEST							
02h	DEVICE ID ("0" "1" "0")			TONE HEADER			MTYPE	MODE
03h		Memory Address (MA21-16)						
04h	Memory Address (MA15-8)							
05h	Memory Address(MA7-0)							
06h	Memory Data(MD7-0)							
08-1Fh	TONE NUMBER (L)							
20-37h	F-NUMBER (L)							TNUM (H)
38-4Fh	BLOCK				PREV	F-NUMBER (H)		
50-67h	TOTAL LEVEL							LDIR
68-7Fh	KEYON	DAMP	LFORST	CH	PAN POT			
80-97h	CHORUS SEND		LFO		VIB			
98-AFh	AR				D1R			
B0-C7h	DL				D2R			
C8-DFh	RATE INTERPOLATION				RR			
E0-F7h	REVERB SEND			-	-	AM		
F8h	-	-	MIX CONTROL (FM-R)			MIX CONTROL (FM-L)		
F9h	-	-	MIX CONTROL (Wave-R)			MIX CONTROL (Wave-L)		
FAh	-	-	-	-	-	-	-	ATC
FBh	-	-	-	-	-	-	-	-

Default :

After initial clear, index 02h becomes 40h (Device ID) and index F8h becomes 2Dh (-15dB), and all the other registers are cleared to "0". For the details of these registers, refer to data sheet for YMF295(OPL4-D).

Note :

BUSY1 is a BUSY flag for Wavetable registers. Wavetable status/Data register is normally accessed by the internal processor.

7. Hardware

7-1. ISA bus interface

(1) Data Bus Connect System

Data BUS

Since driving current of data bus, ADB7-0 pins, of YMF721(OPL4-ML2) is about 2 mA (at VDD = 5.0 V), it is recommended to use bus buffer such as LS245 as necessary. At this time, connect ABDIR pin which outputs bus direction signal of YMF721(OPL4-ML2) with DIR (direction) pin of the bus buffer such as LS245.

RESET

Reset (RST) pin of YMF721(OPL4-ML2) can be made "H" active or "L" active. When using "H" active reset, /RESETSEL pin should be open or set to "H", or to "L" when using "L" active reset. /RESETSEL pin has a built-in pull-up resistor. When this pin is set to "L", the power consumption increases approximately by 30uA from the one obtained when the pin is open or set to "H".

I/O Channel Ready

In normal operation, the internal data bus of YMF721 (OPL4-ML2) connects the built-in processor and FM/Wavetable synthesizer blocks. Every time the ISA bus accesses the register for FM/Wavetable, an internal arbitration circuit causes the internal bus to connect ISA bus and FM/Wavetable synthesizer blocks. YMF721 (OPL4-ML2) uses I/O channel ready (ARDY pin) as the internal arbitration circuit. Connect ARDY pin of YMF721 (OPL4-ML2) and IOCHRDY pin of ISA bus. Although ARDY pin is an open drain output, it is not necessary to attach pull up resistor because it is usually pulled up at the ISA bus.

(2) No Data Bus Connect System

The input pins ADB7-0, A2-0, /MPUCS, /OPLCS, /IOW and /IOR must be pulled up externally. Output pins AIRQ, ABDIR and ARDY pins must be open.

7-2. MIDI interface

When using MPU port of YMF721 (OPL4-ML2), RXD and FSP pins must be pulled up. When using MPU port of the system and receiving MIDI data through RXD pin, FSP pin must be made "L".

7-3. Serial audio interface

YMF721 (OPL4-ML2) outputs clock signals of CLKO (384 fs = 16.9344 MHz), BCO (48 fs = 2.1168 MHz), LRO (fs = 44.1 kHz) and WCO (2 fs = 88.2 kHz) as the serial audio interface. It also outputs four types of data including DO0 (FM external out), DO1 (Wavetable external out), DO2 (MIX out) and DO3 (effect-send out). Normally, it uses the output of DO2. When YMF721 (OPL4-ML2) is in power down mode, /PDOUT pin outputs "L" which can be used as the power down control signal for peripheral systems.

7-4. Others

Power Supply

It is recommended to install a line noise filter in the YMF721 (OPL4-ML2). Be sure to install 0.1uF ceramic capacitor between each of VDD pins and VSS pins as close to the pins as possible, especially the pin No. 63 (VDD).

5V/3V

When operating YMF721 (OPL4-ML2) with 5 V, 5V/3V pin must be pulled up. When operating it with 3.3 V, set the pin to "L".

XI, XO

YMF721 (OPL4-ML2) requires the clock frequency of 33.8688 MHz. This signal can be supplied from the system or from the self-oscillation circuit connected with crystal oscillator

Yamaha recommends either of the following two types of parallel resonance type oscillator made by Daishinku Co., Ltd.

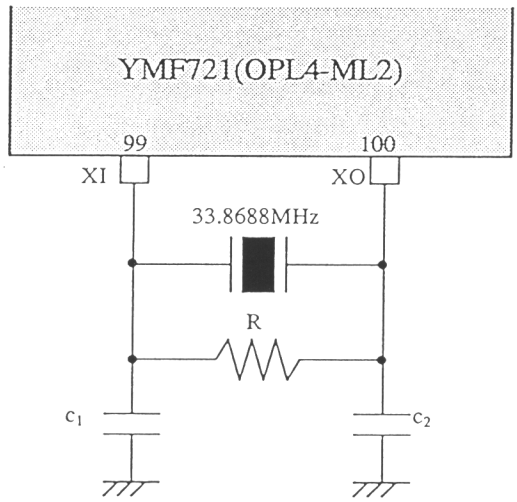
(i) 3rd Overtone Type

AT-49, SMD-49 : R=5.6K, c_1=c_2=10pF

(ii) Fundamental Type

AT-49, SMD-49 : R=1M, c_1=c_2=5pF

Use of the Crystal oscillator with frequency deviation within 100 ppm is recommended. Length of wiring lead from XI and XO pin to each component (crystal, resistor and capacitor) should be 0.5 inch or less respectively and the circuit pattern should be shielded on its periphery to minimize effect on the peripheral devices.



Since YMF721 (OPL4-ML2) is able to use power down mode, the power consumption can be minimized when generation of the clock signal is discontinued during this mode.

7. Hardware

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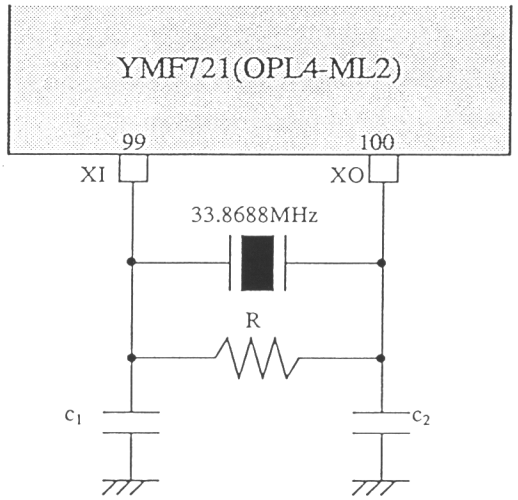
Use of the Crystal oscillator with frequency deviation within 100 ppm is recommended. Length of wiring lead from XI and XO pin to each component (crystal, resistor and capacitor) should be 0.5 inch or less respectively and the circuit pattern should be shielded on its periphery to minimize effect on the peripheral devices.



Since YMF721 (OPL4-ML2) is able to use power down mode, the power consumption can be minimized when generation of the clock signal is discontinued during this mode.

■ Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Minimum	Maximum	Unit
Power Supply Voltage (Analog/Digital)	V_{DD}	V_{SS}-0.5	V_{SS}+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.3	V_{DD}+0.3	V
Input Current	I_{IN}	-20	20	mA
Storage Temperature	T_{STG}	-50	125	℃

Notes : V_{DD}=DV_{DD}=AV_{DD}, V_{SS}=DV_{SS}=AV_{SS}=0[V]

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Operating voltage 1 (5.0V Spec. 5V/3V="H")	V_{DD1}	4.75	5.00	5.25	V
Operating voltage 2 (3.3V Spec. 5V/3V="L")	V_{DD2}	3.00	3.30	3.60	V
Operating Ambient Temperature	T_{OP}	0	25	70	℃

Notes : DV_{SS}=AV_{SS}=0[V]

DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
TTL-Input Pins						
High Level Input Voltage 1	V_{IH1}	Except XI and 5V/3V pins	2.0			V
Low Level Input Voltage 1	V_{IL1}				0.8	V
CMOS-Input Pins						
High Level Input Voltage 1	V_{IH2}	Applicable to XI and 5V/3V	0.7V_{DD}			V
Low Level Input Voltage 1	V_{IL2}				0.2V_{DD}	V
Input Leakage Current	I_L	V_{IN}=V_{SS},V_{DD}	-10		10	μA
Input Capacitance	C_I				10	pF
Pull up Register	R_{UI}	/TEST, /TEST2 /TEST3, /TESTA /TESTB, /RESETSEL	50		400	kΩ
High Level Output Voltage 1	V_{OH1}	I_{OH1} = -80 μA (5V/3V="L")	2.4			V
Low Level Output Voltage 1	V_{OL1}	I_{OL1} = 2mA (*1)			0.4	V
High Level Output Voltage 2	V_{OH2}	I_{OH2} = -80 μA (5V/3V="H")	V_{DD}-1.0			V
Low Level Output Voltage 2	V_{OL2}	I_{OL2} = 2mA (*1)			V_{SS}+0.4	V
Low Level Output Voltage 3	V_{OL}	I_{OL1} = 4mA (5V/3V="L") (*2)			0.4	V
Low Level Output Voltage 4	V_{OL}	I_{OL1} = 12mA (5V/3V="H") (*2)			0.4	V
Output Capacitance	C_O				10	pF

Notes : V_{SS}=0[V], T_{OP}=0～70℃, V_{DD}=5.0±0.25[V]

*1) Applicable to output pins except XO and /ARDY.

*2) Applicable to /ARDY pin.

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AC Characteristics

1. CPU interface (Refer to Fig. 1, 2, 3)

Item	Symbol	Min.	Typ.	Max.	Unit
Address set up to /IOW, /IOR active	t_{AS}	30			ns
Address hold to /IOW, /IOR inactive	t_{AH}	10			ns
/IOW Write Pulse Width	t_{WW}	50			ns
Write Data set up to /IOW active	t_{WDS}	10			ns
Write Data hold to /IOW inactive	t_{WDH}	10			ns
/IOR Read Pulse Width	t_{RW}	80			ns
Read Data access time	t_{ACC}			60	ns
Read Data hold from /IOR inactive	t_{RDH}	10			ns
Chip select setup time	t_{CS}	5			ns
Chip select hold time	t_{CH}	10			ns
RESET Pulse Width	t_{RST}	100			ms

Notes : V_{SS}=0[V], T_{OP}=0～70℃, V_{DD}=5.0±0.25[V]

2. Serial audio interface (Refer to Fig. 4.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKO frequency	f_{CLKO16}		-	16.9344	-	MHz
CLKO duty	D_{CLKO16}		40	50	60	%
BCO frequency	f_{BCK}		-	2.1168	-	MHz
BCO duty	D_{BCLK}		40	50	60	%
Serial data setup time	t_{DS}	BCO ↑ /DO3-0	-	118	-	ns
Serial data hold tim	t_{DH}	BCO ↓ /DO3-0	-	118	-	ns
LRO setup time	t_{LRS}	BCO ↑ /LRO	-	118	-	ns
LRO hold time	t_{LRH}	BCO ↓ /LRO	-	118	-	ns
WCO setup time	t_{WCS}	BCO ↑ /WCO	-	118	-	ns
WCO hold time	t_{WCH}	BCO ↓ /WCO	-	118	-	ns

Notes : V_{SS}=0[V], T_{OP}=0～70℃, V_{DD}=5.0±0.25[V]

Sampling frequency (fs) is 44.1 kHz. Duty factor is measured at 1/2 V_{DD}

3. Others

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Master Clock Frequency	f_{33}	V_{DD}=5.0±0.25[V]		33.8688		MHz
(X'tal 33) Duty	D_{f33}	V_{DD}=3.3±0.3[V]	40	50	60	%
Power Consumption	I_{OP1}	V_{DD}=5.25[V]		40	50	mA
(during normal operation)	I_{OP2}	V_{DD}=3.60[V]		25	30	mA
Power Consumption	I_{OP3}	V_{DD}=5.25[V]		25	50	μA
(during power down mode)	I_{OP4}	V_{DD}=3.60[V]		15	30	μA

Notes : V_{SS}=0[V], T_{OP}=0～70℃

/RESETSEL = "H". Duty factor is measured at 1/2 V_{DD}

I/O write cycle

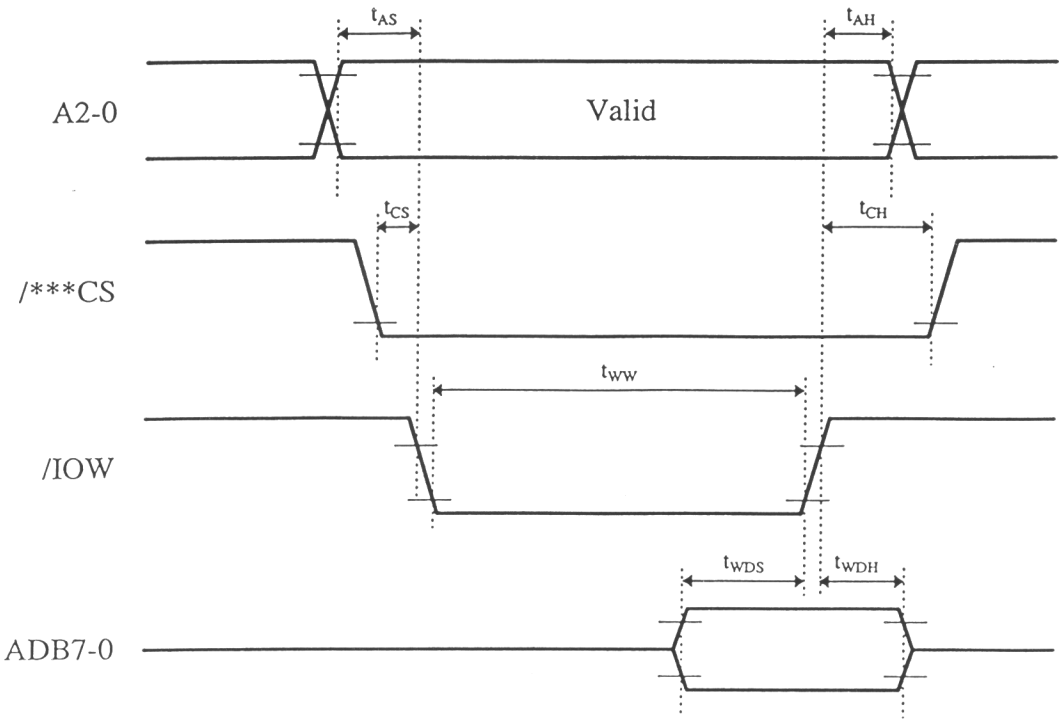


Fig.1

I/O read cycle

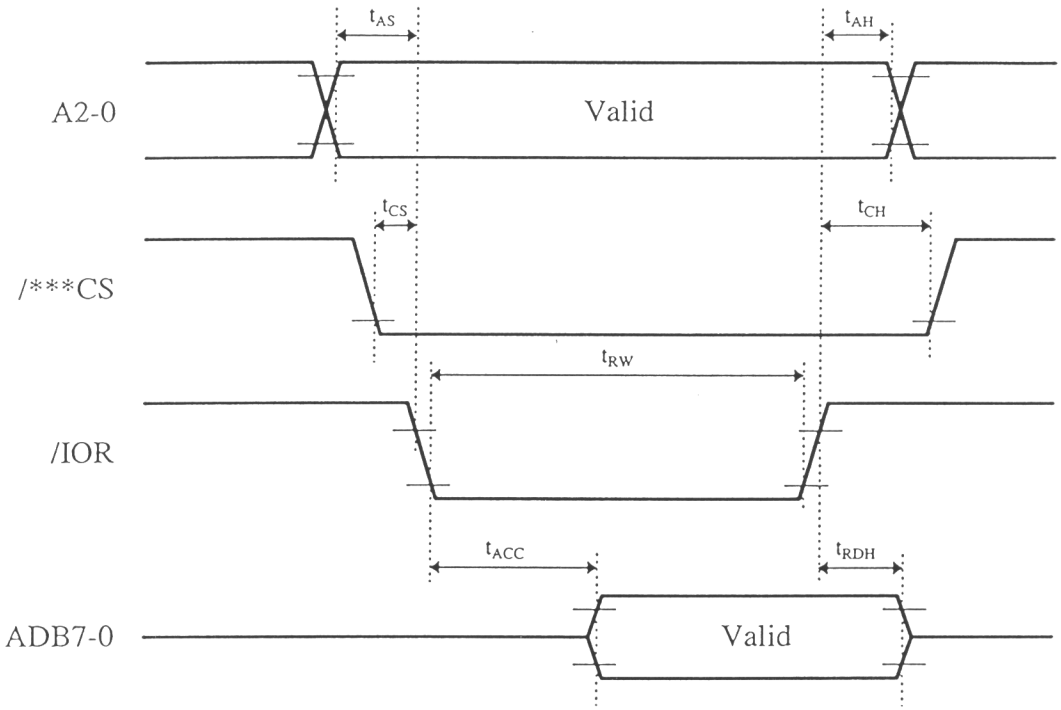


Fig.2

Reset pulse width

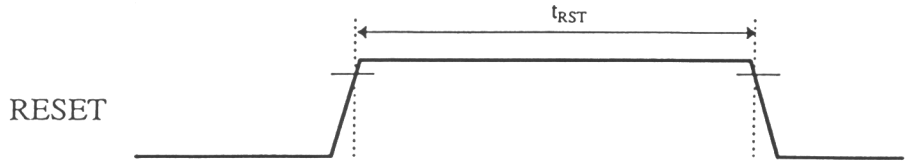


Fig.3

Serial audio interface

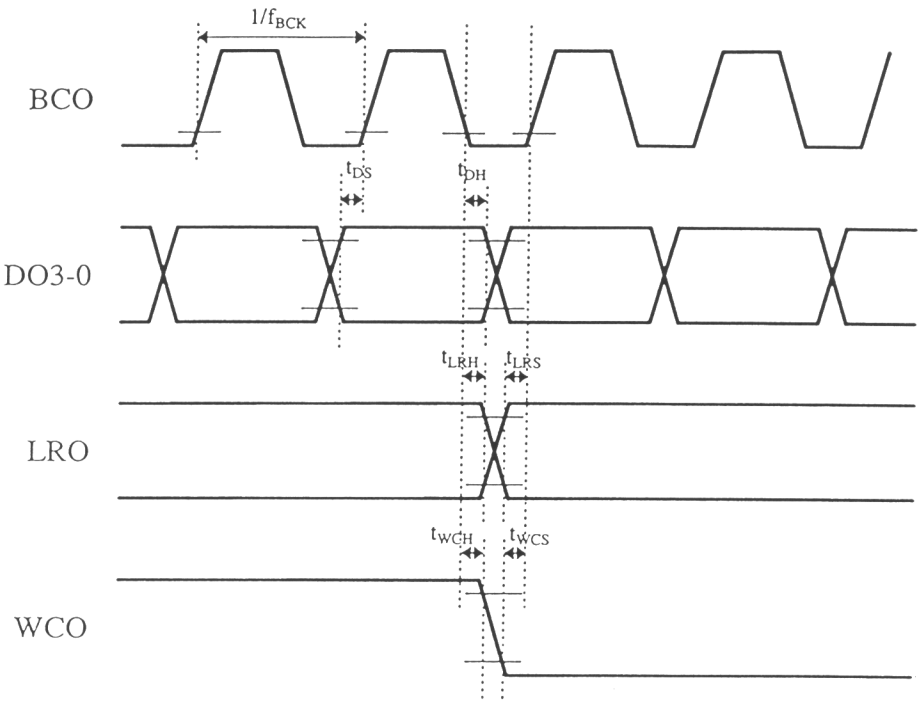


Fig.4

I/O write cycle

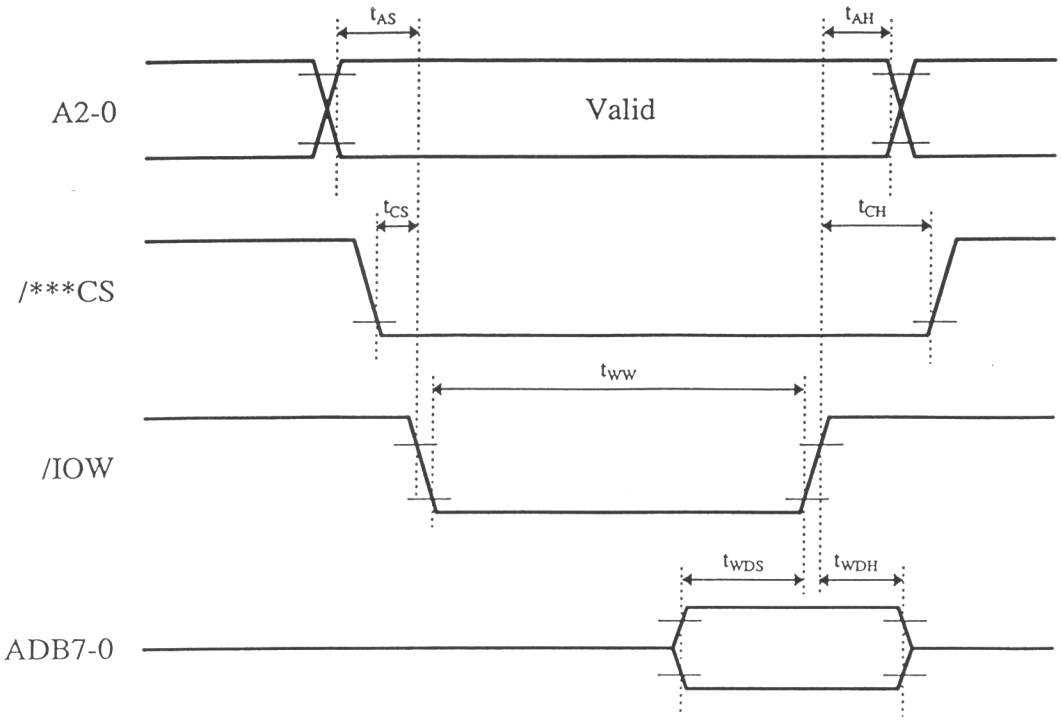


Fig.1

I/O read cycle

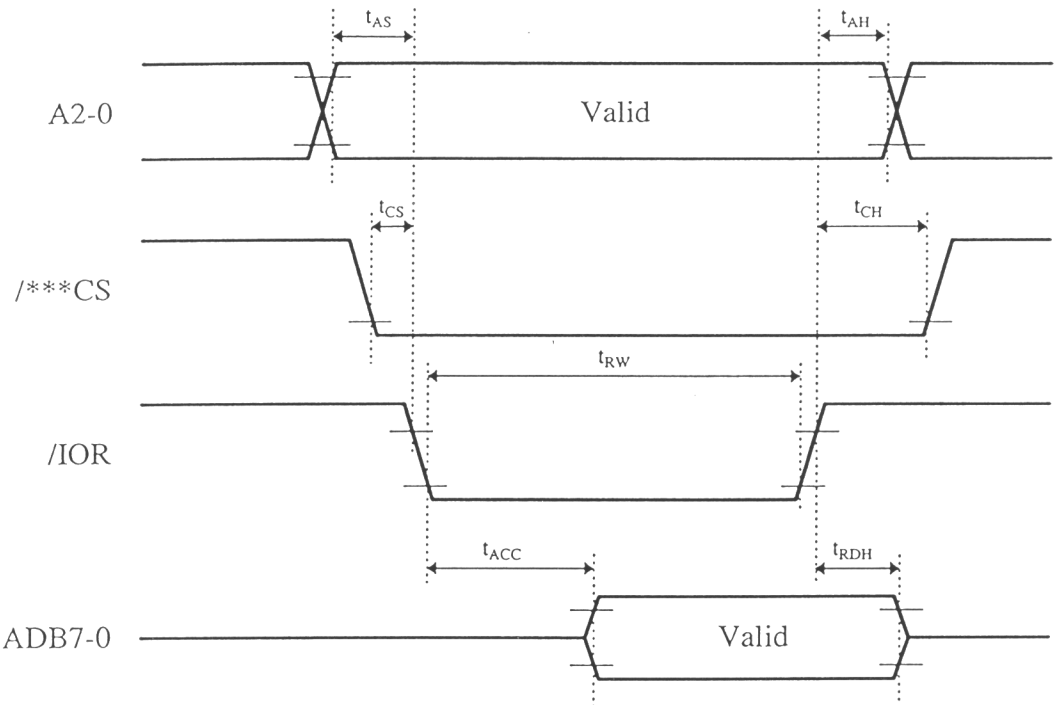


Fig.2

Reset pulse width

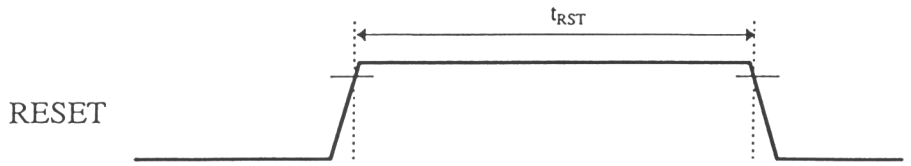


Fig.3

Serial audio interface

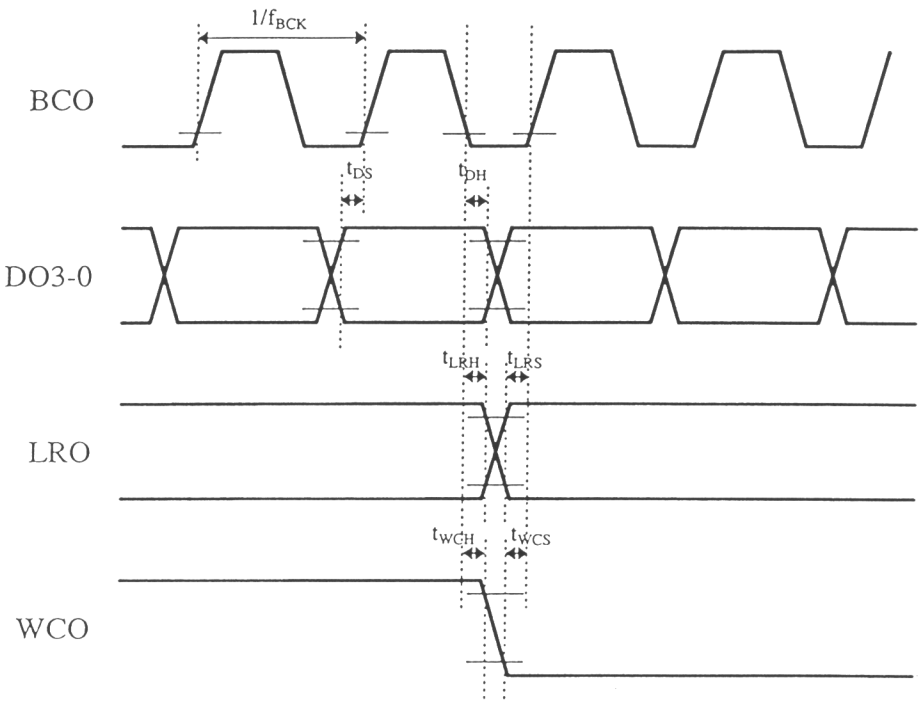


Fig.4

■ Supplementary Information (about commands)

The following commands are used to check existence and identification of YMF704C/721(OPL4-ML/ML2) by using device driver.

Command	Sub Command	Command Length	Response Length	Function
80h	00h	3byte	11byte	Get Processor Device ID
80h	01h	3byte	5byte	Get Processor Software Version
80h	02h	3byte	6byte	Get Processor Software Capacity
81h	00h	3byte	8byte	Get OPL4-MLx Information
82h	00h	3byte	31byte	Get wave ROM Copyright Data
82h	01h	3byte	5byte	Get wave ROM Version

Command 80h

This command is used mainly to obtain version information of the internal processor. The device driver is able to know capability of the internal processor before it controls the hardware.

Sub Command 00h : Get Processor Device ID

Command		Response	
80h	Command byte	8Ah	Response 1st byte
00h	Sub Command	47h "G"	ID Strings
00h	Check sum	4Dh "M"	
		50h "P"	
		5Fh "_"	
		4Fh "O"	
		50h "P"	
		4Ch "L"	
		34h "4"	
		00h	Strings Last Code
		1Eh	Check sum

The character string "GMP_OPL4" is read from ID strings. Existence of YMF721 (OPL4-ML2) can be confirmed with this character string.

Sub Command 01h : Get Processor Software Version

Command		Response	
80h	Command byte	84h	Response 1st byte
01h	Sub Command	02h	Integer part of version number
7Fh	Check sum	00h	1st decimal place of version number
		00h	2nd decimal place of version number
		7Eh	Check sum

Version number of firmware stored in the internal processor is read out as shown below.

YMF704 (OPL4-ML) : Version 1.22

YMF704B(OPL4-ML) : Version 1.23

YMF704C(OPL4-ML) : Version 1.24

YMF721 (OPL4-ML2) : Version 2.00

Sub Command 02h : Get Processor Software Capacity

Command		Response	
80h	Command byte	85h	Response 1st byte
02h	Sub Command	00h	No use
7Eh	Check sum	00h	No use
		00h	No use
		07h	Capacity code
		79h	Check sum

The capacity of internal processor can be known through the capacity code.

bit0 = 1 : The synthesizer is able to add effects such as reverb or chorus send level 1.

bit1 = 1 : Suspend/Resume is supported.

bit2 = 1 :Power down is supported.

YMF704 (OPL4-ML) : Capacity Code=01h

YMF704B(OPL4-ML) : Capacity Code=03h

YMF704C(OPL4-ML) : Capacity Code=03h

YMF721 (OPL4-ML2) : Capacity Code=07h

Command 81h

Sub Command 00h : Get OPL4-MLx Information

Since the synthesizer of YMF721(OPL4-ML2) is the same as YMF295(OPL4-D), the character string of "OPL4D" is obtained as described below.

Command		Response	
81h	Command byte	87h	Response 1st byte
00h	Sub Command	4Fh "O"	ID Strings
00h	Check sum	50h "P"	
		4Ch "L"	
		34h "4"	
		44h "D"	
		00h	Strings Last Code
		1Dh	Check sum

Command 82h

These commands are used to know information about the internal Wavetable sample ROM.

Sub Command 00h : Get Wave ROM Copyright Data

Command		Response	
82h	Command byte	9Eh	Response 1st byte
00h	Sub Command	strings	Copyright Data
00h	Check sum	00h	Strings Last Code
		46h	Check sum

This command is used to know capacity of internal processor. As the strings, character strings of "copyright yamaha corporation"(28bytes) are returned.

Sub Command 01h : Get Wave ROM Version

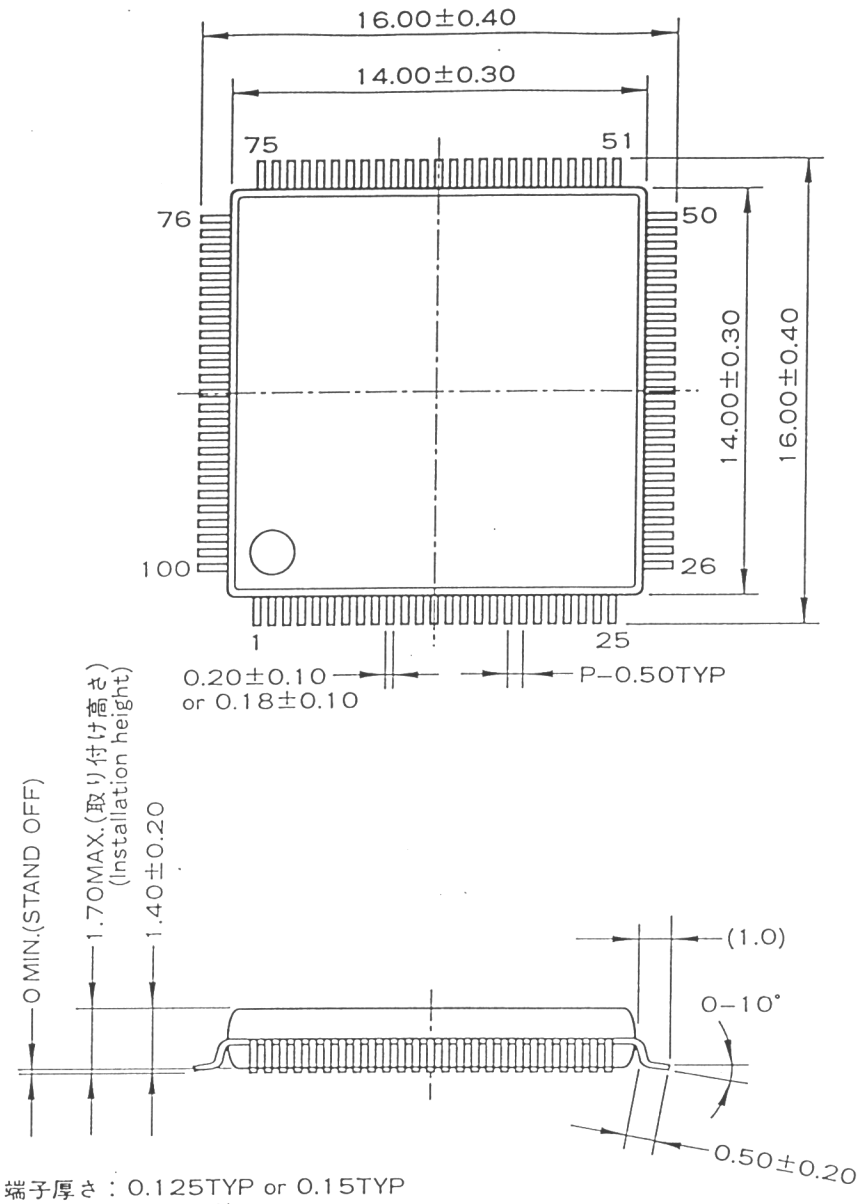
Command		Response	
82h	Command byte	84h	Response 1st byte
01h	Sub Command	01h	Integer part of version number
7Fh	Check sum	00h	First decimal place of version number
		03h	Second decimal place of version number
		7Ch	Check sum

This command is used to know version number of internal Wavetable sample ROM.

YMF704C(OPL4-ML) : Version 1.02

YMF721 (OPL4-ML2) : Version 1.03

■ EXTERNAL DIMENSIONS OF PACKAGE



端子厚さ：0.125TYP or 0.15TYP
(LEAD THICKNESS)

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

Note : LSIs to be installed on the surface of the printed circuit board require special care in storage and soldering. Consult your dealer for the details.

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