Crystal Semiconductor

PCI Audio Design Guide for Embedded Systems

Specification of Hardware Interfaces Required for PCI Audio in Embedded Applications

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Embedded Audio Design Guide for Crystal Semiconductor PCI Audio Devices

1 Revision History

Revision	*Release Date*	*Description*
0.3	1/18/99	Add Revision History section. Describe how to: 1. Stop and start DMA. 2. Control playback volume and capture level.
0.4	1/22/99	Add sections on GPIO pins and EEPROM interface.
0.5	1/29/99	Add description of DMA count playback parameter (PDTC). Change parameter used to control playback volume.
0.6	3/23/99	Correct description of how to set capture sample rate.

2 Introduction

The purpose of this document is to describe how to design device drivers for a Crystal Semiconductor PCI audio device on an embedded platform. Currently, there are two parts that may be part of an embedded PCI audio design, the CS4280 and the CS4281. The CS4280 has been available since September, 1998 while the CS4281 will be available in 1999. The main difference between the two parts is that the CS4280 contains a programmable core while the CS4281 is a pure “hard gate” implementation. Both parts provide full-duplex audio (ie, simultaneous play and capture) and an AC97 CODEC interface.

Crystal Semiconductor also provides the AC97 CODEC to which the PCI audio devices connect. The CS4297 is AC97 Rev. 1.03 compliant with stereo DAC and stereo ADC. The CS4294 is AC97 Rev. 2.1 compliant with quad DAC and stereo ADC.

3 CS4280

3.1 PCI Device Enumeration and Resource Allocation

The PCI BIOS or the OS must enumerate the CS4280 and assign two base memory addresses and one interrupt. The BIOS or OS must also set the *Memory Space Enable*

and *Bus Master Enable* bits in the *Command* register of the *PCI Configuration Space* of the CS4280.

When the CS4280 is enumerated, the OS will load the corresponding driver and the driver will proceed with initialization.

3.2 Initialization

3.2.1 Clocks and PLL

The CS4280 has two clock domains. The PCI interface and most of the registers operate off of the PCI clock. The processor core and the ROM and RAM operate off of a PLL which is driven by the 12.288 MHz AC-link bit clock. The driver is responsible for programming the PLL.

As stated above, the 4280 depends on the AC 97 for clocking. Therefore, the first thing that happens during initialization is starting the bit clock of the AC 97. Once this is done, the PLL is powered up. After the PLL stabilizes, the clock to the 4280 core is enabled.

3.2.2 AC 97 link

After the 4280 core clock is enabled, the AC link is programmed to accept commands across slots one and two (eg, read/write register), send ADC data across the link on input slots three and four, and accept data for the DAC on output slots three and four.

3.2.3 Processor Initialization/Start-up

During hardware/power up reset, the processor is clocked to “flush out” any intermediate states. After reset is complete, the processor clock is stopped (the RUN bit in SPCR is 0 = processor stopped). Initialization and start-up of the processor can be accomplished by the following procedure.

3.2.3.1 Processor Start-up Procedure (after hardware reset)

1. Load processor code image through BA1 memory poke mechanism.

2. Load processor data image through BA1 memory poke mechanism

3. Load frame timer count register (FRMT) with desired value.
   FRMT ← 0xADF.

4. Set RUN, RUNFR, and DRQEN bits in SPCR.
   SPCR ← 0x25.

5. Monitor RUNFR bit in SPCR for 1 to 0 transition.

6. Monitor SPRUN bit in SPCS for 0 to 1 transition (processor is now running).

3.2.4 Processor Software Reset

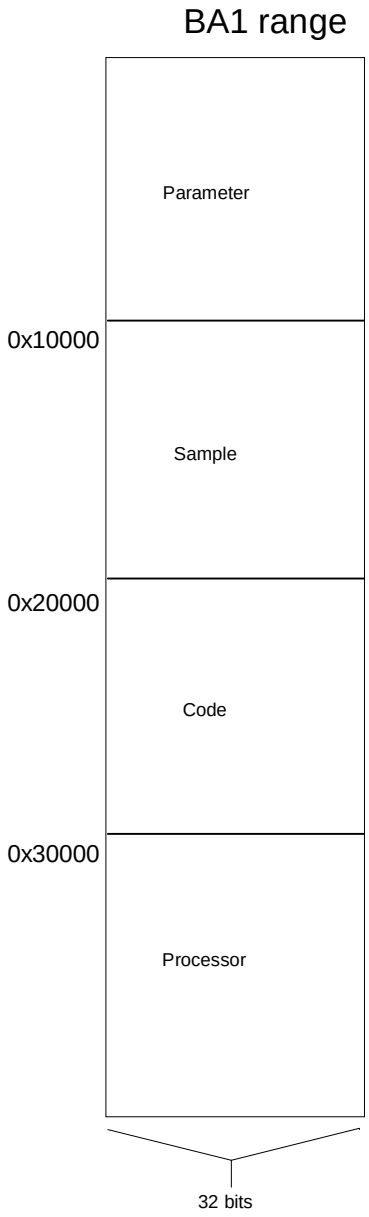
The processor can be reset at any time by software by using the soft reset bit in SPCR.

3.2.4.1 Processor Soft Reset Procedure

1. Set RSTSP bit in SPCR (also clear RUN, RUNFR, and DRQEN).
2. (Processor will immediately be reset.)
3. Clear RSTSP bit in SPCR.
4. (Processor will be reset but stopped with RUN bit=0.)

3.2.5 Code and Data Images

The CS4280 requires a code and data download in order to provide digital audio playback and capture. The memory where the images are stored is mapped into the BA1 memory space of the CS4280. There are actually three separate memories mapped into this space, parameter, sample, and code.



The CS4280's three memories are mapped into the device's BA1 space. Parameter memory starts at byte offset 0 of the BA1 range, memory starts at byte offset 0x10000, and code memory starts at byte 0x20000. Also, there are processor registers mapped into the BA1 beginning at offset 0x30000.

- Figure 1

Parameter memory will be initialized to the extent possible at compile time (ie, the provided image file will contain data as well as code). However, parameter memory also includes variables that are unknown at compile time like the physical addresses of the play and capture buffers and the play and capture sample rates. See Parameter Description for descriptions of the variables used to specify these quantities and the relative locations of these variables.

3.2.6 Initialization Sequence

1. Start PLL out in known state.
   CLKCR1 ← 0.

2. Start serial ports out in known state.
   SERMC1 ← 0.

3. Specify type of CODEC by writing SERACC.
   SERACC ← 0x8 for AC 97 1.03.
   SERACC ← 0x9 for AC 97 2.0.

4. Reset CODEC.
   ACCTL ← 0.
   Delay 100us.
   ACCTL ← 0x1.

5. Enable AC-link sync generation.
   ACCTL ← 0x3.
   Delay 50ms.

6. Set the serial port timing configuration.
   SERMC1 ← 0x2.

7. Setup clock control.
   PLLCC ← 0x7E.
   PLLM ← 0x3A.
   CLKCR2 ← 0x8.

8. Power up the PLL.
   CLKCR1 ← 0x10.
   Delay 50ms.

9. Turn on clock.
   CLKCR1 ← 0x30.

10. Configure the serial port.
    SERC1 ← 0x3.
    SERC2 ← 0x3.
    SERMC1 ← 0x3

11. Wait for CODEC ready.
    While !(ACCSTS & 0x1).

12. Assert valid frame signal.
    ACCTL ← 0x7.

13. Wait for valid AC 97 input slots.
    While (ACISV != 0x3).

14. Set AC 97 output slot valid signals.
    ACOSV ← 0x3.

15. Load code and data images.

16. Save playback parameter, PCTL, and capture parameter, CCTL for use later to start playback or capture DMA, respectively. Then write zero to these locations. (This ensures that DMA doesn't immediately occur upon starting the processor core.)

17. Start the processor core.
    See Processor Start-up Procedure (after hardware reset).

3.3 Digital Audio Playback and Capture

The CS4280 readily supports the standard wave and DirectSound™ API's. The CS4280 provides the "ping-pong" interrupts that the wave API requires. Also, the CS4280 provides the address of the next DMA transfer, which is critical to the DirectSound™ API.

3.3.1 DMA buffer size = 4KB

Larger buffers require the use of the scatter/gather feature of the CS4280 DMA controller. Using scatter/gather adds considerable complexity and isn't necessary if an interrupt rate as high as 100/second (each direction) is acceptable.

3.3.2 Starting and Stopping DMA

The CS4280 contains a DMA controller capable of simultaneously transferring playback and capture data. The DMA controller initiates DMA transfers in order to fill the sample memory buffer used for playback and empty the sample memory buffer used for capture. The following procedure should be used to initiate playback DMA:

1. Program PBA with the address of the source buffer in host memory containing the play data.
2. Program PFIE with the format of the play data and to cause playback interrupts, if desired.
3. Program PSRC and PPI to correspond to the sample rate of the play data.
4. Program PCTL with the contents of PCTL found in the original data image.

Use the following procedure for capture:

1. Program PBA with the address of the destination buffer in host memory that will contain the capture data.
2. Program CIE to cause capture interrupts, if desired.
3. Program CSRC, CD, CCI, and CPI to correspond to the sample rate of the capture data.
4. Program CCTL with the contents of CCTL found in the original data image.

Playback and capture DMA will stop when PCTL and CCTL are written with zero, respectively. Note that playback and capture are entirely independent: either one can occur with or without the other. (See Parameter Description.)

3.3.3 Data Format and Sample Rate

The sample rate and the data format determine the transfer rate of the data in each direction. The play data may be either 8- or 16-bit and either stereo or mono. The capture data format must be 16-bit stereo. The play and capture sample rates may be independent. The playback rate may range from 8000 Hz to 48000 Hz and the capture rate from11025 Hz to 48000 Hz, both with a resolution of 1 Hz. The capture and play sample rates and play format should only be changed when the corresponding DMA transfers have been stopped.

3.3.3.1 Sample Rate Calculation

The play and capture sample rates are each characterized by several values. Both play and capture sample rates have a phase increment that corresponds to the sample rate itself and a correction. The correction prevents error from accumulating over time. The capture sample rate also requires the specification of a sample rate-dependent coefficient increment and delay. The formulas used to calculate the play and capture sample rates are given below.

For capture, the following equations are used:

capture_coefficient_increment = - round(OutputHz * 128 * 65536 / 48000)

capture_phase_increment = floor(48000 * 65536 * 1024 / OutputHz)

cx = round(48000 * 65536 * 1024 – capture_phase_increment * OutputHz)

cy = floor(cx / 200)

capture_sample_rate_correction = cx - 200 * cy

capture_delay = ceil(24 * 48000 / OutputHz)

capture_num_triplets = floor(65536 * OutputHz / 24000)

capture_group_length = 24000 / GCD(OutputHz, 24000)

capture_coefficient_increment, capture_phase_increment, and capture_num_triplets are 32-bit signed quantities. capture_sample_rate_correction, capture_group_length are 16-bit signed quantities and capture_delay is a 14-bit unsigned quantity. (GCD = Greatest Common Divisor)

For play, use the following:

play_phase_increment = floor(InputHz * 65536 * 1024 / 48000)

px = round(InputHz * 65536 * 1024 – play_phase_increment * 48000)

py = floor(px/ 200)

play_sample_rate_correction = px - 200 * py

play_phase_increment is a 32-bit signed quantity. play_sample_rate_correction is a16-bit signed quantity.

3.3.3.2 Length of PCI Bursts

The CS4280 DMA controller transfers digital audio data in bursts. The length of the burst depends on the format of the data being transferred and the size of the sample buffer

used to hold the data. For capture, the data format is always 16-bit, stereo and the size of the capture buffer is fixed so the length of the PCI bursts for capture is fixed at 14.

For playback, the size of the buffer used is fixed but the format of the data is programmable. The buffer has to be big enough to hold the 16-bit, stereo version of the play data, so the length of the PCI burst is varied to accomplish this. See Playback DMA Transaction Count (PDTC) for details on varying the length of the PCI bursts during playback.

3.3.4 Playback Volume and Capture Level

PVOL and CVOL control playback volume and capture level, respectively. The volume is controlled with 16-bit resolution with a value of 8000h corresponding to 0 dB and FFFFh to -85 dB. Unlike the sample rates and play format, PVOL and CVOL may be written while DMA is occurring.

Registers also exist in the AC97 CODEC that can affect the playback volume and capture level. The designer is free to use the AC97 registers or PVOL and CVOL in parameter memory or a combination of both.

3.4 Interrupts

3.4.1 General Description

The CS4280 interrupt controller receives interrupt requests from multiple sources inside the device and presents a single interrupt line (INTA) to the host system. Interrupt controller registers in the CS4280 provide the host interrupt service routine (ISR) with source identification and methods for clearing sources and indicating end-of-interrupt (EOI).

3.4.2 Interrupt Line Control

A master interrupt enable bit, INTENA, controls assertion of the CS4280 interrupt line (INTA) at a global level. When INTENA is clear, no interrupt will be generated as a result of interrupt sources going active. When INTENA is set any interrupt source assertion will generate an external interrupt.

3.4.2.1 INTENA

INTENA is set (interrupts are enabled) by the following condition:

1) EOI command received (to HICR register)

INTENA is cleared (interrupts are disabled) by any one of the following conditions:

1) Host read of HISR (only if any interrupt source bits set, therefore interrupt active) Note that if HISR is read with no interrupt source bits set, INTENA will be unaffected.

2) Explicit clear by write to HICR command register

3) Device hardware reset

3.4.3 Play and Capture Interrupts

If INTENA is set and the playback interrupt is enabled, then once playback DMA is started, playback interrupts will occur after the transfer of every two kilobytes of play data. Specifically, the CS4280 DMA controller will generate a playback interrupt whenever the address of the playback data currently being transferred is a multiple of 2048. Capture interrupts work in exactly the same way; ie, if INTENA is set and the capture interrupt is enabled, then capture interrupts will occur every two kilobytes.

As stated above, the CS4280 has a single interrupt line (INTA). However, play and capture interrupts can still be independently enabled and identified (see Host Interrupt Status Register (HISR)).

3.5 Analog Mixing

See CS4297, 4298, and CS4294 datasheets.

3.6 Parameter Description

This section describes the locations in parameter memory that must/can be changed by the device driver. Except for locations where all 32 bits are specified, the following memory locations may only be modified using a read-modify-write approach (ie, read the location, change the specified bits as desired, and write the result back to the location).

3.6.1 Playback Parameters

Playback DMA Transaction Count (PDTC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						CNT9	CNT8	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

Address: BA1: 00C0h, Read-Write

Definition: This memory location controls the number of DWORDs per play DMA transaction (burst).

Bit Descriptions:

CNT[9:0] Count: Number of DWORDs per play DMA transaction minus one.
00Fh = 16-bit stereo playback data format.
007h = 8-bit stereo or 16-bit mono playback data format.
003h = 8-bit mono playback data format.

Playback Format and Interrupt Enable (PFIE)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PF3	PF2	PF1	PF0							PIE5	PIE4	PIE3	PIE2	PIE1	PIE0

Address: BA1: 00C4h, Read-Write

Definition: This memory location controls the play format and whether the playback interrupt is enabled.

Bit Descriptions:

PIE[5:0] Playback Interrupt Enable:
0 0 0 0 0 0 = Playback interrupt enabled
0 1 0 0 0 0 = Playback interrupt disabled

PF[3] Playback Format, Signed/Unsigned:
0 = No effect.
1 = Each 16-bit word being written will have its most significant bit inverted, to convert incoming unsigned audio data to signed format, or vice-versa.

PF[2] Playback Format, Big/Little-Endian:
0 = No effect.
1 = Each 16-bit word being written will have its low and high bytes swapped, to convert incoming bytewise big-endian audio to little-endian, or vice-versa.

PF[1] Playback Format, Mono/Stereo:
0 = No effect.
1 = Each 16-bit word of audio data is duplicated (written twice) to convert mono audio data to stereo format.

PF[0] Playback Format, 8/16 Bit:
0 = No effect.
1 = Each byte of audio data is padded on the least-significant end with a zero byte, to form a 16-bit word.
To understand the exact transformation that will occur for different combinations of these bits, imagine each of the four operators functioning independently, in the order given above. First, 8-bit data will be converted to 16-bit, then mono data will be duplicated to stereo data. Next, the bytes of each word will be exchanged to convert between little/big endian data, and finally the most significant bit of each resulting word will be inverted to convert between signed and unsigned formats. Any combination of these four operators can be turned on or off, but the requested functions will always operate in this sequence. If all four bits are set to zero, data will be written as-is, with no conversion.

Playback Buffer Address (PBA)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Address: BA1: 00C8h, Read-Write

Definition: This memory location contains the starting physical address of the playback DMA buffer. This buffer must be 4 kilobytes long and the starting address must be a multiple of 4 kilobytes.

Bit Descriptions:

A[31:0] Address: PCI bus address of the start of the playback DMA buffer.

Playback Volume (PVOL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LVOL15	LVOL14	LVOL13	LVOL12	LVOL11	LVOL10	LVOL9	LVOL8	LVOL7	LVOL6	LVOL5	LVOL4	LVOL3	LVOL2	LVOL1	LVOL0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RVOL15	RVOL14	RVOL13	RVOL12	RVOL11	RVOL10	RVOL9	RVOL8	RVOL7	RVOL6	RVOL5	RVOL4	RVOL3	RVOL2	RVOL1	RVOL0

Address: BA1: 00F8h, Read-Write

Definition: This memory location controls the volume level of playback data.

Bit Descriptions:

LVOL[15:0] Left volume: Volume level of left channel of playback data.
8000h = 0dB
FFFFh = -85dB

RVOL[15:0] Right volume: Volume level of right channel of playback data.
8000h = 0dB
FFFFh = -85dB

Playback Sample Rate Correction (PSRC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Address: BA1: 0288h, Read-Write

Definition: This memory location contains the correction factor used during playback sample rate conversion. It ensures that error doesn't accumulate over time.

Bit Descriptions:

C[15:0] Correction: playback_sample_rate_correction (see Sample Rate Calculation).

Playback Control (PCTL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CTL15	CTL14	CTL13	CTL12	CTL11	CTL10	CTL9	CTL8	CTL7	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Address: BA1: 02A4h, Read-Write

Definition: This memory location controls whether playback DMA occurs.

Bit Descriptions:

CTL[15:0] Control: Controls whether playback DMA occurs.
Write zero to stop playback DMA. To start playback DMA, write the data originally contained in the data image in PCTL (see Initialization Sequence).

Playback Phase Increment (PPI)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Address: BA1: 02B4h, Read-Write

Definition: This memory location contains the phase increment used during playback sample rate conversion.

Bit Descriptions:

I[31:0] Increment: playback_phase_increment (see Sample Rate Calculation).

3.6.2 Capture Parameters

Capture Control (CCTL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTL15	CTL14	CTL13	CTL12	CTL11	CTL10	CTL9	CTL8	CTL7	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0

Address: BA1: 0064h, Read-Write

Definition: This memory location controls whether capture DMA occurs.

Bit Descriptions:

CTL[15:0] Control: Controls whether capture DMA occurs.
Write zero to stop capture DMA. To start capture DMA, write the data originally contained in the data image in CCTL (see Initialization Sequence).

Capture Interrupt Enable (CIE)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										CIE5	CIE4	CIE3	CIE2	CIE1	CIE0

Address: BA1: 0104h, Read-Write

Definition: This memory location controls whether the capture interrupt is enabled.

Bit Descriptions:

CIE[5:0] Capture Interrupt Enable:
0 0 0 0 0 1 = Capture interrupt enabled
0 1 0 0 0 1 = Capture interrupt disabled

Capture Buffer Address (CBA)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Address: BA1: 010Ch, Read-Write

Definition: This memory location contains the starting physical address of the capture DMA buffer. This buffer must be 4 kilobytes long and the starting address must be a multiple of 4 kilobytes.

Bit Descriptions:

A[31:0] Address: PCI bus address of the start of the capture DMA buffer.

Capture Sample Rate Correction (CSRC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Address: BA1: 02C8h, Read-Write

Definition: This memory location contains the correction factor used during capture sample rate conversion. It ensures that error doesn't accumulate over time.

Bit Descriptions:

C[15:0] Correction: capture_sample_rate_correction (see Sample Rate Calculation).

Capture Coefficient Increment (CCI)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Address: BA1: 02D8h, Read-Write

Definition: This memory location contains the coefficient increment used during capture sample rate conversion.

Bit Descriptions:

I[15:0] Correction: capture_coefficient_increment (see Sample Rate Calculation).

Capture Delay (CD)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Address: BA1: 02E0h, Read-Write

Definition: This memory location contains the sample delay used for capture sample rate conversion.

Bit Descriptions:

D[13:0] Delay: capture_delay (see Sample Rate Calculation).

Capture Phase Increment (CPI)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Address: BA1: 02F4h, Read-Write

Definition: This memory location contains the phase increment used during capture sample rate conversion.

Bit Descriptions:

I[31:0] Increment: capture_phase_increment (see Sample Rate Calculation).

Capture Group Length (CGL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0

Address: BA1: 0134h, Read-Write

Definition: This memory location contains the group length used during capture.

Bit Descriptions:

L[15:0] Length: capture_group_length (see Sample Rate Calculation).

Capture Number of Triplets (CNT)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
N31	N30	N29	N28	N27	N26	N25	N24	N23	N22	N21	N20	N19	N18	N17	N16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

Address: BA1: 0340h, Read-Write

Definition: This memory location contains the number of sample triplets used during capture.

Bit Descriptions:

N[31:0] Number: capture_num_triplets (see Sample Rate Calculation).

Capture Group Count (CGC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0

Address: BA1: 0138h, Read-Write

Definition: This memory location contains the group length used during capture.

Bit Descriptions:

L[15:0] Length: capture_group_length (see Sample Rate Calculation).

Capture Volume (CVOL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LVOL15	LVOL14	LVOL13	LVOL12	LVOL11	LVOL10	LVOL9	LVOL8	LVOL7	LVOL6	LVOL5	LVOL4	LVOL3	LVOL2	LVOL1	LVOL0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RVOL15	RVOL14	RVOL13	RVOL12	RVOL11	RVOL10	RVOL9	RVOL8	RVOL7	RVOL6	RVOL5	RVOL4	RVOL3	RVOL2	RVOL1	RVOL0

Address: BA1: 02F8h, Read-Write

Definition: This memory location controls the volume level of capture data.

Bit Descriptions:

LVOL[15:0] Left volume: Volume level of left channel of capture data.
8000h = 0dB
FFFFh = -85dB

RVOL[15:0] Right volume: Volume level of right channel of capture data.
8000h = 0dB
FFFFh = -85dB

3.7 Register Descriptions

3.7.1 General Configuration Registers

Serial Port Master Control Register 1 (SERMC1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										XLB	PLB	PTC2	PTC1	PTC0	MSPE

Address: BA0: 420h, Read-Write

Default: 00000000h

Definition: This register provides a host port for configuration and control of the CS4280 serial ports, setting up the master timing configuration.

Bit Descriptions:

MSPE — Master Serial Port Enable: This bit is the master enable/disable for all CS4280 serial port functions. Normally this bit will only be set after all the other serial port configuration registers are initialized.
0 = All serial ports disabled (reset default)
1 = Serial ports enabled as specified in their individual SERC registers (see below)

PTC[2:0] — 0 0 1 = Configuration C: AC 97 link mode, BITCLK in, ASYNC out

PLB — Primary Port Internal Loop Back: This bit controls the internal loopback of SDOUT to SDIN.
0 = Loopback disabled (reset default)
1 = SDOUT to SDIN loopback enabled

XLB — External Loop Back: This bit controls the pin level loopback of SDIN to SDOUT.
0 = Loopback disabled (reset default)
1 = SDIN to SDOUT loopback enabled

Serial Port Configuration Register 1 (SERC1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												SO1F2	SO1F1	SO1F0	SO1EN

Address: BA0: 428h, Read-Write

Default: 00000000h

Definition: This register controls the configuration of the primary output port.

Bit Descriptions:

SO1EN Primary Output Port Enable
0 = Port disabled, no shifts, SDOUT locked low (reset default)
1 = Port enabled

SO1F[2:0] 0 0 1

Serial Port Configuration Register 2 (SERC2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												SI1F2	SI1F1	SI1F0	SI1EN

Address: BA0: 42Ch, Read-Write

Default: 00000000h

Definition: This register controls the configuration of the primary input port.

Bit Descriptions:

SI1EN Primary Input Port Enable.
0 = Port disabled, no shifts, SDIN ignored (reset default)
1 = Port enabled

SI1F[3:0] 0 0 1

3.7.2 AC 97 Registers

AC 97 Control Register (ACCTL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									TC	ASYN	CRW	DCV	VFRM	ESYN	RSTN

Address: BA0: 460h, Read-Write

Default: 00000000h

Definition: This register provides the host control port for the AC 97 link.

Bit Descriptions:

RSTN Reset NOT!: This bit controls the ARST# pin. Note the negative sense of the bit, which matches the active low output pin definition.
0 = ARST# active, AC 97 codec reset (reset default)
1 = ARST# inactive, AC 97 codec not reset.

ESYN Enable Sync: This bit controls ASYNC generation for the AC 97 link (the ASYNC/FSYNC pin).
0 = ASYNC generation disabled (reset default)
1 = ASYNC generation enabled, AC 97 framing will start (FIFO accesses and data shifting will not start until host bypass or processor start)

VFRM Valid Frame: This bit controls “valid frame” value in the AC 97 output stream (the ASDOUT/SDOUT pin).
0 = Valid frame disabled (reset default)
1 = Valid frame enabled, AC 97 codec can interpret frame time slots

DCV Dynamic Command Valid: This bit controls dynamic command address and data generation on the AC 97 link. To generate a valid command data slot:
1) Write the ACCAD and ACCDA registers
2) Clear the TC bit.
3) Set this bit
4) The serial port will dynamically set the slot valid bits for the command address and data slots
5) The serial port will shift out command address and data during their corresponding time slots
6) The serial port will clear this bit, DCV, and the TC bit automatically to indicate completion of the process

CRW Control Read/Write: This bit indicates type of transaction requested to the AC 97 codec control registers.
0 = Write command
1 = Read command

ASYN Asynchronous ASYNC Assertion: This bit allows the unclocked assertion of the ASYNC pin for AC 97 link management protocol requirements.
0 = Normal ASYNC generation (reset default)
1 = Force ASYNC valid (with no clocking dependencies other than PCI clock)

TC 0

AC 97 Status Register (ACSTS)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													WKUP	VSTS	CRDY

Address: BA0: 464h, Read-Only

Default: 00000000h

Definition: This register provides a status port for the AC 97 link (the ASDIN/SDIN pin).

Bit Descriptions:

CRDY Codec Ready: This bit returns the last frame's "codec ready" indicator in the AC 97 input data stream.
0 = Codec not ready
1 = Codec ready

VSTS Valid Status: This set/reset bit support dynamic status capture from the AC 97 input data stream, according to the following rules:
1) A valid status data slot (slot 2 tag) in a given input frame will set this bit
2) The status address and data will be stored in the ACSAD and ACSDA registers
3) Subsequent valid status address and data slots will be ignored until the current set is read
4) Read ACSAD and ACSDA registers upon seeing this bit set
5) Read of the ACSDA register will automatically clear/reset this bit

WKUP Wakeup: This bit indicates that a CS4298 codec attached to the ASDIN/SDIN or ASDIN2 pin signaled a wake-up event by forcing a low-to-high transition on ASDIN/SDIN or ASDIN2 while the AC 97 link is down. When host driver software receives an indication that the CS4280 caused a PCI bus wake-up event by asserting PME#, it should read ACSTS and check this bit to see if the codec was the source of the wake-up event. This bit remains set until host driver software issues a warm reset of the AC 97 link by setting the ASYN bit in ACCTL; specifically, the falling edge of the ASYNC/FSYNC warm reset pulse clears this bit.
0 = No wake-up event signaled by a CS4298 attached to ASDIN/SDIN or ASDIN2
1 = Wake-up event signaled by a CS4298 attached to ASDIN/SDIN or ASDIN2; automatically cleared by a warm reset of the AC 97 link (in turn caused by setting the ASYN bit in ACCTL)

AC 97 Output Slot Valid Register (ACOSV)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						SLV12	SLV11	SLV10	SLV9	SLV8	SLV7	SLV6	SLV5	SLV4	SLV3

Address: BA0: 468h, Read-Write

Default: 00000000h

Definition: This register provides a port for setting the static slot valid signals for the AC 97 tag phase (slot 0) on the AC 97 link (the ASDOUT/SDOUT pin).

Bit Descriptions:

SLV[12:3] Slot Valid bits: These bits set the static slot valid bits in the AC 97 output data stream.
0 = Slot not valid
1 = Slot valid

AC 97 Command Address Register (ACCAD)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									CI6	CI5	CI4	CI3	CI2	CI1	CI0

Address: BA0: 46Ch, Read-Write

Default: 00000000h

Definition: This register provides the host port for setting the command address field for an AC 97 frame on the AC 97 link (the ASDOUT/SDOUT pin). Note that the contents of this register will not be sent out in an output frame unless the dynamic command valid bit is set in ACCTL.

Bit Descriptions:

CI[6:0] Control Register Index: This 7 bit field addresses the 64 16-bit registers in the AC 97 control register address space. Normally bit 0 should always be set to 0 (even addresses only).

AC 97 Command Data Register (ACCDA)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

Address: BA0: 470h, Read-Write

Default: 00000000h

Definition: This register provides the host port for setting the command data field for an AC 97 frame on the AC 97 link (the ASDOUT/SDOUT pin). Note that the contents of this register will not be sent out in an output frame unless the dynamic command data valid bit is set in ACCTL.

Bit Descriptions:

CD[15:0] Control Register Data: This 16 bit field provides data during writes to the AC 97 control register address space. This field should be set to 0000h during control register reads.

AC 97 Input Slot Valid Register (ACISV)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						ISV12	ISV11	ISV10	ISV9	ISV8	ISV7	ISV6	ISV5	ISV4	ISV3

Address: BA0: 474h, Read-Only

Default: 00000000h

Definition: This register provides a port for sensing the input slot valid signals for the AC 97 tag phase (slot 0) on the AC 97 link (the ASDIN/SDIN pin). The contents of this register are dynamic updated with each AC 97 input frame.

Bit Descriptions:

ISV[12:3] Slot Valid bits: These bits sense the slot valid bits in the AC 97 input data stream.
0 = Slot not valid
1 = Slot valid

AC 97 Status Address Register (ACSAD)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									SI6	SI5	SI4	SI3	SI2	SI1	SI0

Address: BA0: 478h, Read-Only

Default: 00000000h

Definition: This register provides a port for capturing the status address field for an AC 97 input frame on the AC 97 link (the ASDIN/SDIN pin). Note that the contents of this register will not be overwritten by another input frame's valid status address unless the valid status bit is cleared in ACSTS by a read of ACSDA.

Bit Descriptions:

SI[6:0] Status Register Index: This 7 bit field returns the captured status address returned in slot 1 of the AC 97 input frame.

AC 97 Status Data Register (ACSDA)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

Address: BA0: 47Ch, Read-Only

Default: 00000000h

Definition: This register provides the host port for capturing the status data field for an AC 97 input frame on the AC 97 link (the ASDIN/SDIN pin). Note that the contents of this register will not be overwritten by another input frame's valid status address unless the valid status bit is cleared in ACSTS by a read of this register.

Side Effect: When this register is read, the valid status bit in ACSTS is cleared.

Bit Descriptions:

SD[15:0] Status Data: This 16 bit field returns data of a read from the AC 97 control register address space.

3.7.3 Clock Control Registers

Clock Control Register 1 (CLKCR1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									PLLOS	SWCE	PLLP	PLLSS1	PLLSS0		

Address: BA0: 400h, Read-Write

Default: 00000000h

Definition: Clock Control Register 1 provides a host port for general device configuration and control.

Bit Descriptions:

PLLSS[1:0] PLL Source Select: This field selects the clock source for the pre-divider and the PLL.
0 0 = Serial Port Bit Clock: For AC97 configuration (reset default).
0 1 = Reserved
1 0 = PCI Bus Clock: For debug and development only.
1 1 = Reserved.

PLLP PLL Power Up: This bit is the master enable/disable for the PLL. Note that "powering up" the PLL requires a certain stabilization delay before operating the device.
0 = Stop PLL (reset default).
1 = PLL running.

SWCE Software Clock Enable: This bit is the master enable/disable for the DMA, RAM, and processor clocks. Clearing this bit without clearing PLLP and OSCP allows a reduced power state without the start-up latency of stopping the crystal oscillator or PLL.
0 = Device clocks stopped (reset default).
1 = Device clocks enabled.

PLLOS PLL Output Select: This bit selects the clock fed to the processor core and DMA/RAM blocks.
0 = Normal PLL output (reset default).
1 = PCI clock (for debug/development only).

Clock Control Register 2 (CLKCR2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												PDIVS3	PDIVS2	PDIVS1	PDIVS0

Address: BA0: 404h, Read-Write

Default: 00000000h

Definition: Clock Control Register 2 provides a host port for general device configuration and control.

Bit Descriptions:

PDIVS[3:0] Pre-divide Select: This field selects the pre-divide for the PLL source.
0 0 1 0 = Reserved
1 0 0 0 = Divide by 8: For AC97 configuration.
0 0 0 0 = Divide by 16: For PCI bus clock sourcing configuration (reset default, debug only).
All Others = Selects programmed number as divider (debug only).

PLL Multiplier Register (PLLM)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								PLLM7	PLLM6	PLLM5	PLLM4	PLLM3	PLLM2	PLLM1	PLLM0

Address: BA0: 408h, Read-Write

Default: 00000000h

Definition: The PLL Multiplier register provides a host port for general device configuration and control.

Bit Descriptions:

PLLM[7:0] 0 0 1 1 1 0 1 0

PLL Capacitor Coefficient Register (PLLCC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								LPF4	LPF3	LPF2	LPF1	LPF0	CDR2	CDR1	CDR0

Address: BA0: 40Ch, Read-Write

Default: 00000000h

Definition: The PLL Capacitor Coefficient register provides a host port for PLL capacitor control for the loop filter and ICO. This capacitor control capability allows a wider range of operation for the device.

Bit Descriptions:

CDR[2:0] 1 1 0

LPF[4:0] 0 1 1 1 1

3.7.4 Processor registers

Processor Control Register (SPCR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									RSTSP	DRQEN			RUNFR	STPFR	RUN

Address: BA1: 30000h, Read-Write

Default: 00000000h

Definition: This register contains control bits for controlling processor behavior and operation, including support for debugging.

Bit Descriptions:

RUN This bit is used as a master run/stop signal for the processor.
0 = Processor is unconditionally stopped (reset default).
1 = Processor is “allowed” to run, subject to control by the other bits in this control register.
Note: A 1 to 0 transition will stop the processor, but may leave the processor in an indeterminate state.

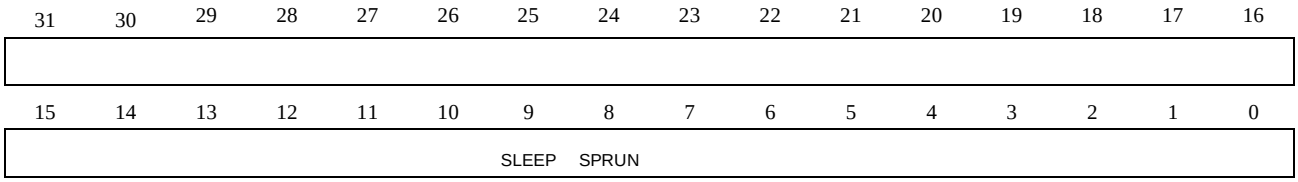
STPFR Stop At Frame: This bit is used to stop the processor at the next frame boundary.
0 = Processor will continue upon reaching frame boundary (reset default).
1 = Processor will stop at next frame.
Note: This bit is “self-clearing”: the bit will transition from 1 to 0 after the stop is executed.

RUNFR Run At Frame: This bit is used to restart processor execution at the next frame boundary.
0 = Processor status/operation unaffected (reset default).
0 to 1 transition = Processor will start execution at next frame boundary.
1 = Processor status/operation unaffected.
Note: This bit is “self-clearing”: the bit will transition from 1 to 0 after the run is executed.

DRQEN DMA Requesting Enable: This bit is used to control ability of the processor’s multi-channel request engine to generate requests. The bit is normally on when the processor is running. DRQEN may be disabled and selectively enabled during debugging to discretely control times that DMA requests may be generated.
0 = New DMA requests disabled (reset default).
1 = New DMA requests enabled.

RSTSP Reset processor: This bit is used for a software controlled reset of the processor. The bit should be set to 1 to initiate a reset, and must be written back to a 0 in order to allow execution after reset. A reset triggered by this bit is equivalent to a hardware reset to the processor.
0 = Processor status/operation unaffected (reset default).
1 = Processor held in reset (as long as bit is active).

Processor Clock Status Register (SPCS)



Address: BA1: 30028h, Read-Only

Default: 00000000h (only sleep is active)

Definition: This is a read-only status register for the processor clock control state machine. It should be monitored after a write to SPCR to detect when processor state actually changes (many state machine transitions happen at frame boundaries).

Bit Descriptions:

SPRUN Processor “Run” Flag: Composite state bit indicating processor run/stop status.
0 = Processor is stopped.
1 = Processor is running.

SLEEP Sleep State (active low bit): If active (0), processor clock stopped (reset state).

Frame Timer Register (FRMT)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FTV15	FTV14	FTV13	FTV12	FTV11	FTV10	FTV9	FTV8	FTV7	FTV6	FTV5	FTV4	FTV3	FTV2	FTV1	FTV0

Address: BA1: 30030h, Read-Write

Default: 00000000h

Definition: The frame timer register provides a host port for setting the frame timer preload value. It can be read or written at any time (regardless of processor run state).

Bit Descriptions:

FTV[15:0] Frame Timer Value: Number of processor clocks between frames.

3.7.5 Interrupt Reporting Registers

Host Interrupt Status Register (HISR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTENA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														CINT	PINT

Address: BA0: 000h, Read-Only

Default: 00000000h

Definition: The Host Interrupt Status register provides interrupt source information to the host interrupt service routine. Reading this register has side effects (see functional description below).

Bit Descriptions:

INTENA Current state of internal interrupt enable bit. First read after interrupt will show INTENA = 1 (not cleared until end of/after read). Subsequent reads of HISR will show INTENA = 0 until EOI issued.

CINT Indicates capture interrupt.

PINT Indicates play interrupt.

Functional Description:

- PINT and CINT are cleared at hardware reset.
- PINT or CINT is set upon receiving a signal from the DMA controller.
- If either interrupt source bit is set and interrupts are enabled, the host interrupt line will be asserted.

Host read of HISR clears all source bits and disables interrupts (sets INTENA to 0) after the read completes.

Host Interrupt Control Register (HICR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														CHGM	IEV

Address: BA0: 008h, Read-Write

Default: N/A

Definition: The Host Interrupt Control register provides a host write port for EOI and discrete masking of interrupts. Also, it provides a read port for INTENA status.

Bit Descriptions:

CHGM INTENA Change Mask: This bit, if set to 1 on a write, enables the writing of the IEV bit into INTENA. If CHGM = 0, then INTENA is unaffected. On a host read this bit always returns a zero.

IEV INTENA Value: On a write, this bit contains the new value of INTENA to be stored if CHGM = 1. On a host read this bit contains the current state of INTENA.

Usage Descriptions:

- EOI command will be a write of 0x00000003 to HICR.
- Interrupt disable command (clear of INTENA) will be a 00000002 write to HICR.
- Read of current value of INTENA (without side effects) will be the value in bit 0 from a read of HICR.

GENERAL PURPOSE INPUT/OUTPUT PINS

Purpose

Some CS4280 device pins are available for general purpose input or output use. Many of these pins are dual function and will not be available in certain system configurations. When available, they can be used for system-defined functionality driven by host software.

Pins for GPIO Use

The following table shows the pins available for GPIO use and the system configurations in which they are available.

Pin Name	Type	Usage	Access
JACX	I/O, open drain	Not available in AC97 configurations where joystick function is used.	JSIO Register, 4A0h
JACY	I/O, open drain	Not available in AC97 configurations where joystick function is used.	JSIO Register, 4A0h
JBCX	I/O, open drain	Not available in AC97 configurations where joystick function is used.	JSIO Register, 4A0h
JBCY	I/O, open drain	Not available in AC97 configurations where joystick function is used.	JSIO Register, 4A0h
JAB1	Input	Not available in joystick configuration or SDO2 aux serial port usage.	JSPT Register, 480h
JAB2	Input	Not available in joystick configuration or SDO3 aux serial port usage.	JSPT Register, 480h
JBB1	Input	Not available in joystick configuration or aux serial port usage with LRCLK required.	JSPT Register, 480h
JBB2	Input	Not available in joystick configuration or aux serial port usage with MCLK required.	JSPT Register, 480h
SDIN2/GPIO	I/O	Not available if auxillary serial input port required.	GPIOR Register, 4B8h
VOLUP/XTALI	Input	Not available if crystal required.	GPIOR Register, 4B8h
VOLDN/XTALO	Input	Not available if crystal required.	GPIOR Register, 4B8h
ARST#	Output	Not available in AC97 configurations.	ACCTL Register, 460h
ARST2#	Output	Not available in dual CS4297 configurations.	ACCTL2 Register, 4E0h
EECLK/GPOUT	Output	Available if no EE required, may be used if EE present and protocol observed.	CFGI Register, 4B0h
EEDAT/GPIO2	I/O, open drain	Available if no EE required, may be used if EE present and protocol observed.	CFGI Register, 4B0h
EGPIO0*	I/O	Available in 128 pin package only.	EGPIO* Registers
EGPIO1*	I/O	Available in 128 pin package only.	EGPIO* Registers
EGPIO2*	I/O	Available in 128 pin package only.	EGPIO* Registers
EGPIO3*	I/O	Available in 128 pin package only; multiplexed with async/sync serial I/O port ASCLK signal.	EGPIO* Registers
EGPIO4*	I/O	Available in 128 pin package only; multiplexed with async/sync serial I/O port ASFCLK signal.	EGPIO* Registers
EGPIO5*	I/O	Available in 128 pin package only; multiplexed with async/sync serial I/O port ASDI signal.	EGPIO* Registers
EGPIO6*	I/O	Available in 128 pin package only; multiplexed with async/sync serial I/O port ASDO signal.	EGPIO* Registers
EGPIO7*	I/O	Available in 128 pin package only.	EGPIO* Registers
EGPIO8*	I/O	Available in 128 pin package only; multiplexed with CLKRUN# signal.	EGPIO* Registers

Host Access Methods

GPIO pins with alternate access ports

See definition of pin control bit in associated register, as shown in table above.

Other GPIO pins

Controlled by GPIOR or EGPIO* registers as defined below.

Register Definitions

General Purpose I/O Register (GPIOR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												SI2OE	SI2D	VOLUP	VOLDN

Address: Host BA0: 4B8h, Read-Write

Default: 00000000h

Definition: The General Purpose I/O register provides a host port for accessing I/O pins not accessible through any other register.

Bit Descriptions:

VOLDN Volume Down Pin Sense: This read-only bit returns the VOLDN pin state.
0 = VOLDN pin is low
1 = VOLDN pin is high

VOLUP Volume Up Pin Sense: This read-only bit returns the VOLUP pin state.
0 = VOLUP pin is low
1 = VOLUP pin is high

SI2D Data SDIN2: This bit represents a host port view of the SDIN2 pin, returning the current state of the pin on reads and setting the pin's state on writes (if output enabled).

SI2OE Output Enable SDIN2: This control bit enables the output buffer on the SDIN2 pin. If this bit is enabled, then writes to the SI2D bit will be presented on the pin.
0 = Output disabled, pin has input function only (reset default)
1 = Output enabled

Extended GPIO Direction Register (EGPIODR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							GPOE8	GPOE7	GPOE6	GPOE5	GPOE4	GPOE3	GPOE2	GPOE1	GPOE0

Address: Host BA0: 4BCh, Read-Write

Default: 00000000h

Definition: The Extended General Purpose I/O Direction Register provides a host port for controlling the direction (input or output) of the extended GPIO pins available only in the 128 pin package.

Bit Descriptions:

GPOE[8:0] These control bits enable the output buffers on the EGPIO[8:0] pins.
0 = Output disabled, pin has input function only (reset default)
1 = Output enabled

Extended GPIO Polarity/Type Register (EGPIOPTR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							GPPT8	GPPT7	GPPT6	GPPT5	GPPT4	GPPT3	GPPT2	GPPT1	GPPT0

Address: Host BA0: 4C0h, Read-Write

Default: 000001FFh

Definition: The Extended General Purpose I/O Polarity/Type Register provides a host Port for controlling the polarity and type of the extended GPIO pins available only in the 128 pin package.

Bit Descriptions:

GPPT[8:0] These bits control the polarity of input pins and the type of output pins.
0 = For input pins, the input is active low; for output pins, the output is CMOS compatible
1 = For input pins, the input is active high; for output pins, the output is an open drain (reset default)

Extended GPIO Sticky Register (EGPIOTR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							GPS8	GPS7	GPS6	GPS5	GPS4	GPS3	GPS2	GPS1	GPS0

Address: Host BA0: 4C4h, Read-Write

Default: 00000000h

Definition: The Extended General Purpose I/O Sticky Register provides a host Port for controlling whether the input pins available only in the 128 pin package are latched (non-sticky is used for level sensitive inputs, sticky for edge sensitive inputs). Sticky bits are cleared by writing zeros to the corresponding positions in the EGPIOSR register.

Bit Descriptions:

GPS[8:0] These bits control whether or not the corresponding input pin is sticky.
0 = Input pin is not sticky
1 = Input pins is sticky

Extended GPIO Wakeup Register (EGPIOWR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							GPW8	GPW7	GPW6	GPW5	GPW4	GPW3	GPW2	GPW1	GPW0

Address: Host BA0: 4C8h, Read-Write

Default: 00000000h

Definition: The Extended General Purpose I/O Wakeup Register provides a host Port for controlling whether the input pins available only on the 128 pin package cause wake up events (assertion of PME# by the PCI interface).

Bit Descriptions:

GPW[8:0] These bits control whether or not the corresponding input pin causes a wake up event.
0 = Input pin does not cause a wake up event
1 = Input pins does cause a wake up event

Extended GPIO Status Register (EGPIOSR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							GPS8	GPS7	GPS6	GPS5	GPS4	GPS3	GPS2	GPS1	GPS0

Address: Host BA0: 4CCh, Read-Write

Default: 00000000h

Definition: The Extended General Purpose I/O Status Register provides a host Port for reading the current status of input pins and writing values to output pins.

Bit Descriptions:

GPS[8:0] These bits control reflect the current status of the EGPIO pins when read and set the value of pins configured for output when written. Writing zero to bits corresponding to input pins configured for "sticky" operation (see the EGPIOTR register) clears the sticky bit.

0 = Pin is inactive

1 = Pin is active

EEPROM CONFIGURATION INTERFACE

General Description

The CS4280 configuration interface allows connection of an external serial EEPROM to the device in order to provide power-up configuration information. There are several master control bits and subsystem identification fields that affect the overall CS4280 configuration.

The external serial EEPROM is not required for proper operation of the device. However, it may be required to support specific operating system compatibility requirements; specifically, Microsoft requires PCI devices to support the configuration space subsystem vendor ID and subsystem ID (there are optional in the PCI 2.1 specification), and if the CS4280 is used on an expansion card, then an external serial EEPROM must be used to load these IDs. If an external serial EEPROM is not present, then the device is configured by default as follows:

CS4280 Default Configuration

- Subsystem ID fields (ID and Vendor ID) report 0000h

After a hardware reset, a state machine in the CS4280 checks the EEPDIS strapping pin. If it's not strapped to VDD, the state machine will load the configuration data, if present (otherwise the two EEPROM interface pins are configured for use as PC/PCI request and grant signals). The EEPROM device is accessible to the host processor for reading/writing via a control register (described below).

External Connection

Presence of the external configuration EEPROM is detected by attempting to load data from it and checking for a valid header. Connection of the device is via 2 pins on the device, EECLK and EEDAT. EECLK is used to provide the serial clock, and EEDAT is used to provide serial data I/O capability.

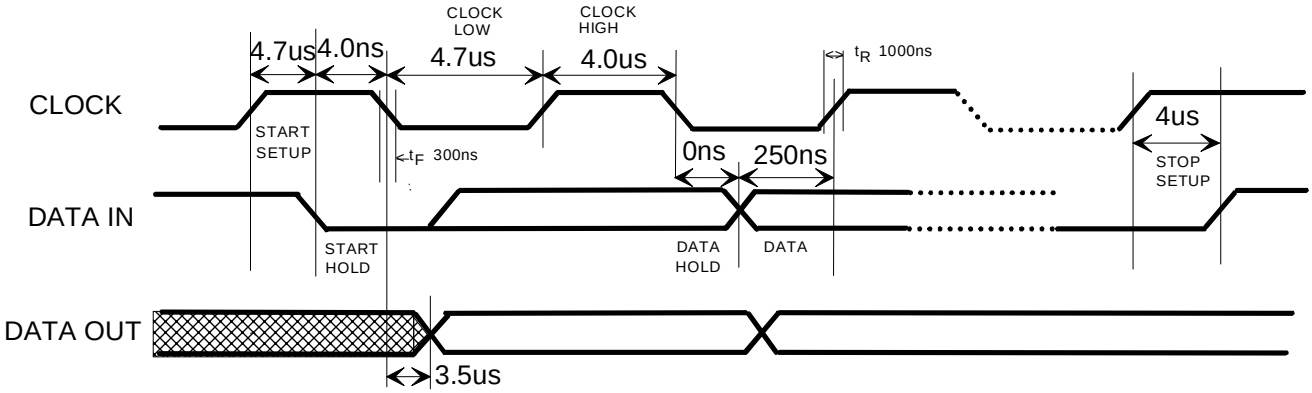
Initialization

On a hardware reset, a hardware-based EEPROM controller steps through the following sequence to initialize the CS4280:

CS4280 Initialization

- Check EEPDIS and ensure it's not strapped to VDD.
- Enable EEPROM interface (switches mode of EECLK pin).
- Send a dummy write to set the byte address to 0.
- Start sequential read of bytes from EEPROM.
- Check signature header as loaded; abort if an invalid signature is detected.
- Load fixed number of bytes, transferring data into destination configuration bits as loaded.

The only time when the CS4280 accesses the EEPROM is after a hardware reset; the CS4280 can only read EEPROM devices — it cannot write them unassisted. Writing a EEPROM can be accomplished through a configuration interface register accessible from the host. The timing of the data and clock signals for the initialization load are generated by a hardware state machine. The minimum timing relationship between the clock and data is shown in the figure below. The state of the data line can change only when the clock line is low. A state change of the data line during the time that the clock line is high is used to indicate start and stop conditions.



The EEPROM device read access sequence is shown in the figure below. The timing follows that of a random read sequence. The CS4280 first performs a dummy write operation, generating a start condition followed by the slave device address and an byte address of zero. The slave address is made up of a device identifier (0xA) and a bank select (bits A2-A0). The bank select bits select among eight 256 byte blocks. The bank select bits may be used to select among multiple 256 byte blocks within a single device, i.e. a 1KB memory may be comprised

of a single 1KB EEPROM with four 256 byte banks. The CS4280 always begins access at byte address zero and continues accessing one byte at a time. The byte address automatically increments by one until a stop condition is detected.

Control Register

The configuration interface register (CFGI) contains the control bits for host software-based manipulation of the external EEPROM (if attached).

Configuration Interface Register (CFGI)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												EELD	DIN/ EEN	DOUT	CLK

Address: BA0: 4B0h, Read-Write

Default: 00000000h

Definition: The Configuration Interface register provides a host port for reading and writing an external serial EEPROM.

Bit Descriptions

CLK — When DIN/EEN is set to a one by the host, the EECLK pin follows the state of this register bit.

DOUT — When DIN/EEN is set to a one by the host, the EEDAT pin follows the state of this register bit.

DIN/EEN — This bit is used to read back data from the EEPROM and to enable the DOUT and CLK bits onto the CS4280 pins. When DIN/EEN is set to a one the DOUT and CLK bits will be enabled onto the EEDAT and EECLK pins.

EELD — This bit is used to indicate if a successful load of initialization data happened after hardware reset.

0 = EEPROM load aborted (EE not present or header mismatch).
1 = EEPROM load successful.

Usage: The CS4280 provides a two wire serial interface that is directly controlled by two register bits. The timing of the two bits is controlled by the host software. One bit is used as a clock (CLK) while the other is used as a data output (DOUT) bit to the EEPROM device.

Host Operation: Reading/Writing

PCI bus access to the EEPROM is enabled via the DIN/EEN bit in the CFGI register. When the DIN/EEN bit is written to a one then the CLK and DOUT bits are enabled on the EECLK and EEDAT pins, respectively. The timing of the clock and data signals is completely

determined by host-based software and should meet the timing requirements as shown previously. In order to read back data from the EEPROM device, the DOUT bit must be set to a one.

Memory Data Format

The following table shows the EEPROM configuration contents. Note the doubleword alignment for configuration space loads.

Byte Offset	Field Description	Configuration Location	Notes
0	Header / Version: Constant 55h	N/A	Abort if <> 55h
1	Primary subsystem vendor ID low byte	Offset 2Ch	
2	Primary subsystem vendor ID high byte	Offset 2Dh	
3	Primary subsystem ID low byte	Offset 2Eh	
4	Primary subsystem ID high byte	Offset 2Fh	
5	Configuration byte 1 for CFL1 register	N/A	Contents defined by driver
6	Configuration byte 2 for CFL2 register	N/A	Contents defined by driver

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