CL-PD6729

Preliminary Data Sheet

FEATURES

- **Single-chip PCMCIA (PC Card) host adapter**
- **Direct connection to PCI bus**
- **Direct connection of two PCMCIA sockets**
- **ZV Port™ support for multimedia applications**
- **Compliant with PCI 2.1**
- **Compliant with PCMCIA 2.1 and JEIDA 4.1**
- **82365SL-compatible register set, ExCA™-compatible**
- **Automatic Low-power Dynamic mode for lowest power consumption**
- **Programmable Suspend mode**
- **Five programmable memory windows per socket**
- **Two programmable I/O windows per socket**
- **Programmable card access cycle timing**
- **8- or 16-bit PCMCIA card support**
- **ATA disk interface support**
- **Automatic flash memory timing support**
- **3.3V, 5V, or mixed 3.3/5V operation**
- **Supports PCMCIA low-voltage card specification**
- **Multiple CL-PD6729s can be used on the PCI bus without external hardware**
- **208-pin PQFP**

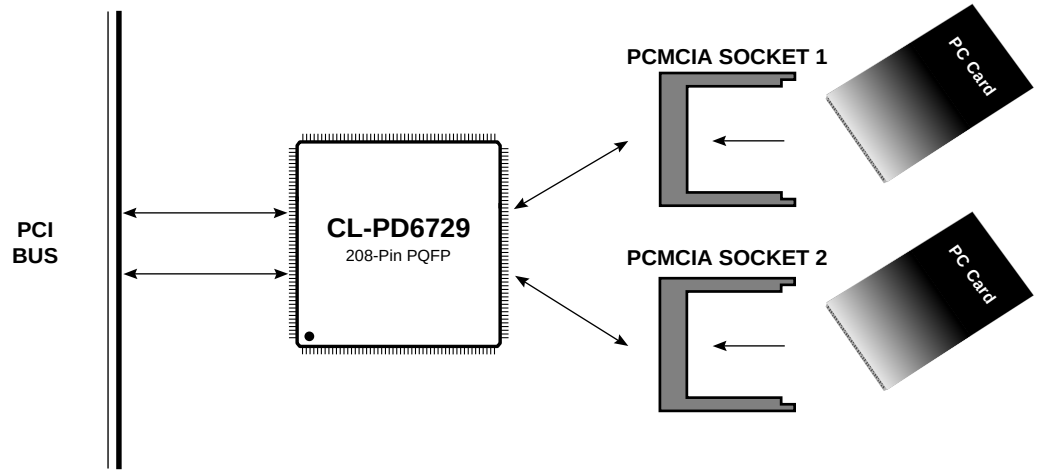
PCI-to-PCMCIA Host Adapter

OVERVIEW

The CL-PD6729 is a single-chip PCMCIA (also known as PC Card) host adapter solution capable of controlling two fully independent PCMCIA sockets. The chip is fully PCMCIA-2.1 and JEIDA-4.1 compliant and is optimized for use in notebook and handheld computers where reduced form factor and low power consumption are critical design objectives. With the CL-PD6729, a complete dual-socket PCMCIA solution with power-control logic can occupy less than 2 square inches (excluding connectors).

The CL-PD6729 chip employs energy-efficient, mixed-voltage technology that can reduce system power consumption by over 50 percent. The chip also provides a Suspend mode, which stops the internal clock, and an automatic Low-power Dynamic mode, which stops transactions on the PCMCIA bus, stops internal clock distribution, and turns off much of the internal circuitry. *(cont.)*

System Block Diagram



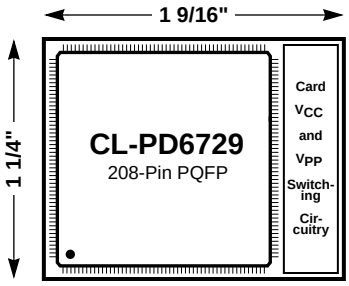
OVERVIEW (cont.)

PC applications typically access PCMCIA cards through the socket/card-services software interface. To assure full compatibility with existing socket/card-services software and PC-card applications, the register set in the CL-PD6729 is a superset of the Intel® 82365SL register set.

The chip provides fully buffered PCMCIA interfaces, meaning that no external logic is required for buffering signals to/from the interface, and power consumption can be controlled by limiting signal transitions on the PCMCIA bus.

Notebook Computer Design Priorities	*Supporting Features*
■ Small Form Factor	❒ Single-chip solution ❒ No external buffers for host or socket interfacing ❒ Efficient board layout
■ Minimum Power Consumption	❒ Automatic Low-power Dynamic mode ❒ Suspend mode ❒ Mixed-voltage operation
■ High Performance	❒ Write FIFO ❒ Programmable timing supports more cards, faster reads and writes
■ Compatibility	❒ Compliant with PCMCIA 2.1 and JEIDA 4.1 ❒ Compliant with PCI 2.0 ❒ 82365SL A-step register-compatible, ExCA™-compatible

Host Adapter Form Factor



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DOCUMENT REVISION HISTORY

Version 2.0

Following are major changes between Version 1.0 of the CL-PD6729 Advance Data Sheet (dated June 1994) and Version 2.0 of the CL-PD6729 Preliminary Data Sheet:

General

The Addendum/Change Notice to the CL-PD6729 Advance Data Sheet Date June 1994 is incorporated in this data sheet.

The following changes are only applicable to CL-PD6729 silicon Revision E or later:

Eight additional operation registers have been added in for device identification.

Two additional bits have been added in for full 3-bit controlled Zoomed Video support.

Timer Clock Divide bit has been deleted. The socket timing clocking is permanently fixed at 1/2 the PCI clock frequency.

GPIO feature has been deleted. AC socket timing parameters have generally changed from number of clock periods minus 10 ns to number of clock periods minus 20 ns.

Section

2 A_VS1/GPSTB1, A_VS2/GPSTB2, B_VS1/GPSTB1, and B_VS2/GPSTB2 pin names in Figure 2-1 are changed to A_VS1, A_VS2, B_VS1, and B_VS2 accordingly. And in Table 2-2, their pin descriptions are changed from I/O type to I type. IRQ[12:9] pin description in Table 2-1 is changed from I/O type to O type.

3.1.2 Figure 3-2 is updated to show that CL-PD6729 decodes the first 64 Kbytes in the PCI bus I/O address space.

3.1.3 A new section is added in for full 3-bit controlled Zoomed Video.

3.1.5 Table 3-1 is updated to more closely reflect expected values.

3.1.11 VS1 and VS2 paragraph is updated with the removal of the GPIO feature.

5.2 DEVSEL# Timing is changed from 01 to 10 to show that CL-PD6729 is a slow-speed PCI device.

5.4 Header Type is changed from 80h to 00h to show that CL-PD6729 is a single-function PCI device.

5.6 Interrupt pin is changed from 00h to 01h to show that CL-PD6729 requests INTA# interrupt during configuration.

6.1 Table 6-1 is updated with the eight additional Operation registers for device identification.

10.1 Misc Control 1 register is updated with the Multimedia Enable bit description.

10.3 Timer Clock Divide bit is removed from the Misc Control 2 register since the PCMCIA interface is set to operate at half the PCI_CLK or EXT_CLK frequency.

10.5 Speaker_Is_LED_Input description is changed.

10.7 External Data (Index 2Fh) register is removed.

Extension Control 2 (Index 2Fh and 6Fh) registers are removed.

10.7.3 Misc Control 3 register is added in for full 3-bit controlled Zoomed Video support.

10.8 A new section is added in for device identification. Eight Operation registers are added.

13.2 Table 13-5 and Table 13-6 are updated to more closely reflect expected values.

13.3.1 DEVSEL# signal in Figure 13-1 is corrected in drawing.

13.3.3 AC socket timing parameters have generally changed from number of clock periods minus 10 ns to number of clock periods minus 20 ns.

Symbol t8 is changed from Tcp+10 (MIN) to Tcp+20 (MAX).

13.3.4 -WAIT signal is added in Figure 13-7, Word I/O Read/Write Timing.

1. GENERAL CONVENTIONS

The following general conventions apply to this document.

Bits within words and words within various memory spaces are generally numbered with a *0* (zero) as the least-significant bit or word. For example, the least-significant bit of a byte is bit 0, while the most-significant bit is bit 7.

In addition, number ranges for bit fields and words are presented with the most-significant value first. Thus, when discussing a bit field within a register, the bit number of the most-significant bit is written first, followed by a hyphen (-) and then the bit number of the least-significant bit; as in, bits 7-0.

In this document, the names of the CL-PD6729 internal registers are bold-faced. For example, **Chip Revision** and **Power Control** are register names. The names of bit fields are written with initial upper-case letters. For example, Card Power On and Battery Voltage Detect are bit field names.

Numbers and Units

The unit *Kbyte* designates 1024 bytes (2^{10}). The unit *Mbyte* designates 1,048,576 bytes (2^{20}). The unit *Gbyte* designates 1,073,741,824 bytes (2^{30}). The unit *Hz* designates hertz. The unit *kHz* designates 1000 hertz. The unit *MHz* designates 1,000,000 Hz. The unit *ms* designates millisecond. The unit μs designates microsecond. The unit *ns* designates nanosecond. The unit *mA* designates milliampere. The unit *V* immediately following a number designates volt.

Hexadecimal numbers are presented with all letters in uppercase and a lowercase *h* appended. For example, *14h* and *03CAh* are hexadecimal numbers.

Binary numbers have the letter *b* appended to them or are enclosed in single quotation marks. For example, *11b* and *'11'* are binary numbers.

Numbers not indicated by an *h* or *b* are decimal.

In addition, a capital letter *X* is used within numbers to indicate digits ignored by the CL-PD6729 within the current context. For example, *101XX01b* is a binary number with bits 3-2 ignored.

2. PIN INFORMATION

The CL-PD6729 device is packaged in a 208-pin PQFP (plastic quad flat pack) or VQFP (very-tight-pitch quad flat pack) component package. The interface pins can be divided into four groups:

- PCI bus interface pins
- PCMCIA socket interface pins (two sets)
- Power control and general interface pins
- Power, ground, and no-connect pins

Refer to Figure 2-1 for the CL-PD6729 pin diagram. The pin assignments for the groups of interface pins are shown in Table 2-1 through Table 2-4.

2.1 Pin Diagram

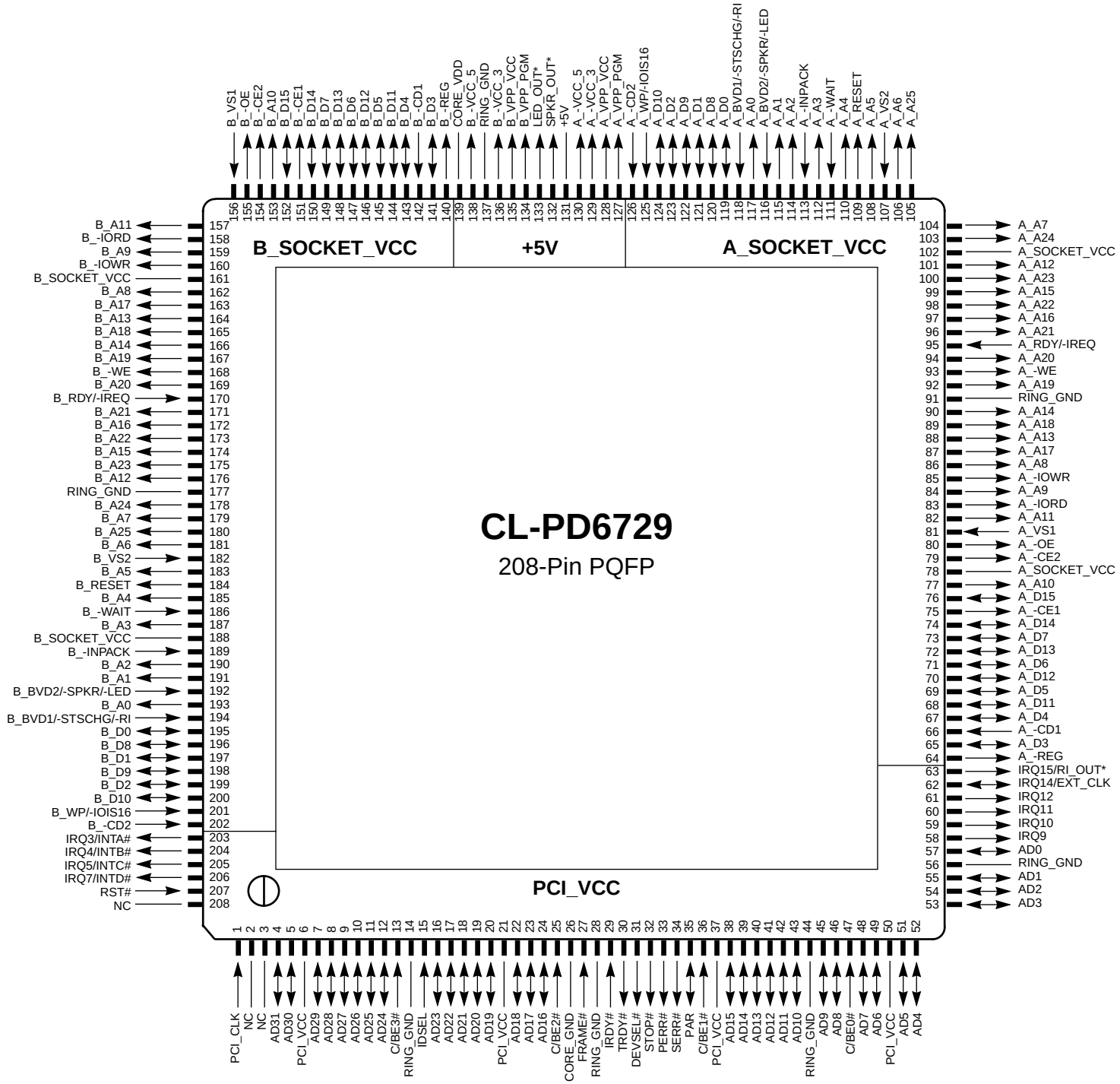


Figure 2-1. CL-PD6729 Pin Diagram

2.2 Pin Description Conventions

The following conventions apply to the pin description tables in Section 2.3:

- A pound sign (#) at the end of a pin name indicates an active-low signal for the PCI bus.
- A dash (-) at the beginning of a pin name indicates an active-low signal for the PCMCIA bus.
- An asterisk (*) at the end of a pin name indicates an active-low signal that is a general-interface for the CL-PD6729.
- Pins marked with a dagger (†) in the pin description tables can be switched between CMOS and TTL input levels when CORE_VDD is powered at 5 volts. All other pins use CMOS input levels when CORE_VDD is powered at 5 volts and TTL input levels when powered at 3.3 volts.
- A pin name ending in bracketed digits separated by a colon [n:n] indicates a multi-pin bus.
- The pin number (Pin Number) column indicates the package pin that carries the listed signal. Note that multi-pin buses are listed with the first pin number corresponding to the most-significant bit of the bus. For example, pin numbers 4-5, 7-12, 16-20, 22-24, 38-43, 45-46, 48-49, 51-55, and 57 associated with PCI Bus Address Input and Data Input/Output pins AD[31:0] indicate that:
  - AD[31] is pin 4
  - AD[1] is pin 55
  - AD[0] is pin 57
- The quantity (Qty.) column indicates the number of pins used (per socket where applicable).
- The I/O-type code (I/O) column indicates the input and output configurations of the pins on the CL-PD6729. The possible types are defined below.
- The power-type code (Pwr.) column indicates the output drive power source for an output pin or the pull-up power source for an input pin on the CL-PD6729. The possible types are defined below.

I/O Type	Description
I	Input pin
I-PU	Input pin with an internal pull-up resistor
O	Constant-driven, output pin
I/O	Input/output pin
OD	Open-drain output pin
TO	Three-state output pin
TO-PU	Three-state output pin with internal pull-up resistor
PW	Power or ground pin

Power Type	Output or Pull-up Power Source
1	+5V: powered from a 5-volt power supply (in most systems, see description of +5V pin in Table 2-4)
2	A_SOCKET_VCC: powered from the Socket A V_{CC} supply connecting to PCMCIA pins 17 and 51 of Socket A
3	B_SOCKET_VCC: powered from the Socket B V_{CC} supply connecting to PCMCIA pins 17 and 51 of Socket B
4	PCI_VCC: powered from the PCI bus power supply
5	CORE_VDD: powered from the lowest available logic supply, which in most systems is 3.3 volts

NOTE: All pin inputs are referenced to CORE_VDD, independently of their output supply voltage.

- The drive-type (Drive) column describes the output drive-type of the pin (see DC specifications in Chapter 13 for more information). Note that the drive type listed for an input-only (I) pin is not applicable (–).

2.3 Pin Descriptions

Table 2-1. PCI Bus Interface Pins

Pin Name	Description	Pin Number	Qty.	I/O	Pwr.	Drive
AD[31:0]	**PCI Bus Address Inputs / Data Input/Outputs:** These pins connect to PCI bus signals AD[31:0].	4-5, 7-12, 16-20, 22-24, 38-43, 45-46, 48-49, 51-55, 57	32	I/O	4	PCI Spec.
C/BE[3:0]#	**PCI Bus Command / Byte Enables:** The command signalling and byte enables are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# are interpreted as the bus commands. During the data phase, C/BE[3:0]# are interpreted as byte enables. The byte enables are to be valid for the entirety of each data phase, and they indicate which bytes in the 32-bit data path are to carry meaningful data for the current data phase.	13, 25, 36, 47	4	I	–	–
FRAME#	**Cycle Frame:** This input indicates to the CL-PD6729 that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is at its final phase.	27	1	I	–	–
IRDY#	**Initiator Ready:** This input indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#.	29	1	I	–	–
TRDY#	**Target Ready:** This output indicates the CL-PD6729's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#.	30	1	TO	4	PCI Spec.
STOP#	**Stop:** This output indicates the current target is requesting the master to stop the current transaction.	32	1	TO	4	PCI Spec.
IDSEL	**Initialization Device Select:** This input is used as a chip select during configuration read and write transactions. This is a point-to-point signal. The CL-PD6729 must be connected to its own unique IDSEL line (from the PCI bus arbiter or one of the high-order AD bus pins).	15	1	I	–	–
DEVSEL#	**Device Select:** The CL-PD6729 drives this output active (low) when it has decoded the PCI address as one that it is programmed to support, thereby acting as the target for the current PCI cycle.	31	1	TO	4	PCI Spec.
PERR#	**Parity Error:** The CL-PD6729 drives this output active (low) if it detects a data parity error during a write phase.	33	1	TO	4	PCI Spec.
SERR#	**System Error:** This output is pulsed by the CL-PD6729 to indicate an address parity error.	34	1	OD	4	PCI Spec.

Table 2-1. PCI Bus Interface Pins *(cont.)*

Pin Name	Description	Pin Number	Qty.	I/O	Pwr.	Drive
PAR	**Parity:** This pin is sampled the clock cycle after completion of each corresponding address or write data phase. For read operations this pin is driven from the cycle after TRDY# is asserted until the cycle after completion of each data phase. It ensures even parity across AD[31:0] and C/BE[3:0]#.	35	1	I/O	4	PCI Spec.
PCI_CLK	**PCI Clock:** This input provides timing for all transactions on the PCI bus to and from the CL-PD6729. All PCI bus interface signals described in this table (Table 2-1), except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of PCI_CLK; and all CL-PD6729 PCI bus interface timing parameters are defined with respect to this edge. This input can be operated at frequencies from 0 to 33 MHz.	1	1	I	–	–
RST#	**Device Reset:** This input is used to initialize all registers and internal logic to their reset states and place most CL-PD6729 pins in a high-impedance state.	207	1	I	–	–
IRQ15/ RI_OUT*	**Interrupt Request 15 / Ring Indicate Out:** This output can be used either as an interrupt output (usually the system's IRQ15 interrupt line), or if **Misc Control 2** register bit 7 is a '1', as a ring indicate output from a socket's BVD1/-STSCHG/-RI input.	63	1	TO	4	2 mA
IRQ14/ EXT_CLK	**Interrupt Request 14 / External Clock:** This pin can be used either as an interrupt output (usually the system's IRQ14 interrupt line), or if **Misc Control 2** register bit 0 is a '1', as an alternate external clock input that will provide the internal clock to the CL-PD6729 for PCMCIA cycle timing when the PCI bus is not active.	62	1	I/O	4	2 mA
IRQ[12:9]	**Interrupt Request:** These outputs indicate programmable interrupt requests generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6729 to the system, a common use is to connect these pins to the corresponding signal name in the system.	61-58	4	O	4	2 mA
IRQ3/INTA#	**Interrupt Request 3 / PCI Bus Interrupt A:** This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6729 to the system, a common use is to connect this pin to the system IRQ3 signal or to the PCI bus INTA# signal.	203	1	O	4	PCI Spec.

Table 2-1. PCI Bus Interface Pins *(cont.)*

Pin Name	Description	Pin Number	Qty.	I/O	Pwr.	Drive
IRQ4/INTB#	**Interrupt Request 4 / PCI Bus Interrupt B:** This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6729 to the system, a common use is to connect this pin to the system IRQ4 signal or to the PCI bus INTB# signal.	204	1	TO	4	PCI Spec.
IRQ5/INTC#	**Interrupt Request 5 / PCI Bus Interrupt C:** This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6729 to the system, a common use is to connect this pin to the system IRQ5 signal or to the PCI bus INTC# signal.	205	1	TO	4	PCI Spec.
IRQ7/INTD#	**Interrupt Request 7 / PCI Bus Interrupt D:** This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the CL-PD6729 to the system, a common use is to connect this pin to the system IRQ7 signal or to the PCI bus INTD# signal.	206	1	TO	4	PCI Spec.
PCI_VCC	**PCI Bus V_{CC}**: These pins can be connected to either a 3.3- or 5-volt power supply. The PCI bus interface pin outputs listed in this table (Table 2-1) will operate at the voltage applied to these pins, independent of the voltage applied to other CL-PD6729 pin groups.	6, 21, 37, 50	4	PW	–	–

Table 2-2. Socket Interface Pins

Pin Name[1]	Description[2]	Pin Number		Qty.	I/O	Pwr.	Drive
		Socket A	Socket B				
-REG	**Register Access:** In Memory Card Interface mode, this output chooses between attribute and common memory. In I/O Card Interface mode, this signal is active (low). In ATA mode this signal is always high.	64	140	1	TO	2 or 3	2 mA
A[25:0]	PCMCIA socket address outputs.	105, 103, 100, 98, 96, 94, 92, 89, 87, 97, 99, 90, 88, 101, 82, 77, 84, 86, 104, 106, 108, 110, 112, 114, 115, 117	180, 178, 175, 173, 171, 169, 167, 165, 163, 172, 174, 166, 164, 176, 157, 153, 159, 162, 179, 181, 183, 185, 187, 190, 191, 193	26	TO	2 or 3	2 mA
D[15:0] †	PCMCIA socket data I/O pins.	76, 74, 72, 70, 68, 124, 122, 120, 73, 71, 69, 67, 65, 123, 121, 119	152, 150, 148, 146, 144, 200, 198, 196, 149, 147, 145, 143, 141, 199, 197, 195	16	I/O	2 or 3	2 mA
-OE	**Output Enable**: This output goes active (low) to indicate a memory read from the PCMCIA socket to the CL-PD6729.	80	155	1	TO	2 or 3	2 mA
-WE	**Write Enable**: This output goes active (low) to indicate a memory write from the CL-PD6729 to the PCMCIA socket.	93	168	1	TO	2 or 3	2 mA
-IORD	**I/O Read**: This output goes active (low) for I/O reads from the socket to the CL-PD6729.	83	158	1	TO	2 or 3	2 mA
-IOWR	**I/O Write**: This output goes active (low) for I/O writes from the CL-PD6729 to the socket.	85	160	1	TO	2 or 3	2 mA

[1] To differentiate the sockets, all socket-specific pins have either A_ or B_ prepended to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.

[2] When a socket is configured as an ATA drive interface, socket interface pin functions change. See Chapter 12.

Table 2-2. Socket Interface Pins *(cont.)*

Pin Name[1]	Description[2]	Pin Number		Qty.	I/O	Pwr.	Drive
		Socket A	Socket B				
WP/-IOIS16 †	**Write Protect / I/O Is 16-Bit**: In Memory Card Interface mode, this input is interpreted as the status of the write protect switch on the PCMCIA card. In I/O Card Interface mode, this input indicates the size of the I/O data at the current address on the PCMCIA card.	125	201	1	I	–	–
-INPACK †	**Input Acknowledge**: The -INPACK function is not applicable in PCI bus environments. It is, however, advisable to connect this pin to the PC Card socket's -INPACK pin.	113	189	1	I-PU	2 or 3	–
RDY/-IREQ †	**Ready / Interrupt Request**: In Memory Card Interface mode, this input indicates to the CL-PD6729 that the card is either ready or busy. In I/O Card Interface mode, this input indicates a card interrupt request.	95	170	1	I-PU	2 or 3	–
-WAIT †	**Wait**: This input indicates a request by the card to the CL-PD6729 to halt the cycle in progress until this signal is deactivated.	111	186	1	I-PU	2 or 3	–
-CD[2:1]	**Card Detect**: These inputs indicate to the CL-PD6729 the presence of a card in the socket. They are internally pulled high to the voltage of the +5V power pin.	126, 66	202, 142	2	I-PU	1	–
-CE[2:1]	**Card Enable**: These outputs are driven low by the CL-PD6729 during card access cycles to control byte/word card access. -CE1 enables even-numbered address bytes, and -CE2 enables odd-numbered address bytes. When configured for 8-bit cards, only -CE1 is active and A0 is used to indicate access of odd- or even-numbered bytes.	79, 75	154, 151	2	TO	2 or 3	2 mA
RESET	**Card Reset:** This output is low for normal operation and goes high to reset the card. To prevent reset glitches to a card, this signal is high-impedance unless a card is seated in the socket, card power is applied, and the card's interface signals are enabled.	109	184	1	TO	2 or 3	2 mA

[1] To differentiate the sockets, all socket-specific pins have either A_ or B_ prepended to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.

[2] When a socket is configured as an ATA drive interface, socket interface pin functions change. See Chapter 12.

Table 2-2. Socket Interface Pins *(cont.)*

Pin Name[1]	Description[2]	Pin Number		Qty.	I/O	Pwr.	Drive
		Socket A	Socket B				
BVD2/-SPKR/ -LED †	**Battery Voltage Detect 2 / Speaker / LED:** In Memory Card Interface mode, this input serves as the BVD2 (battery warning status) input. In I/O Card Interface mode, this input can be configured as a card's -SPKR binary audio input. For ATA or non-ATA (SFF-68) disk-drive support, this input can also be configured as a drive-status LED input.	116	192	1	I-PU	2 or 3	–
BVD1/ -STSCHG/-RI †	**Battery Voltage Detect 1 / Status Change / Ring Indicate:** In Memory Card Interface mode, this input serves as the BVD1 (battery-dead status) input. In I/O Card Interface mode, this input is the -STSCHG input, which indicates to the CL-PD6729 that the card's internal status has changed. If bit 7 of the **Interrupt and General Control** register is set to a '1', this pin serves as the ring indicate input for wakeup-on-ring system power management support.	118	194	1	I-PU	2 or 3	–
VS2	**Voltage Sense 2:** This pin is used in conjunction with VS1 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the +5V power pin. This pin should be connected to PCMCIA socket pin 57.	107	182	1	I	1	–
VS1	**Voltage Sense 1:** This pin is used in conjunction with VS2 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the +5V power pin. This pin should be connected to PCMCIA socket pin 43.	81	156	1	I	1	–
SOCKET_VCC	This pin can be connected to either a 3.3- or 5-volt power supply. The socket interface outputs (listed in this table, Table 2-2) will operate at the voltage applied to these pins, independent of the voltage applied to other CL-PD6729 pin groups. Connect these pins to the V_{CC} supply of the socket (pins 17 and 51 of the respective PCMCIA socket).	78, 102	161, 188	2	PW	–	–

[1] To differentiate the sockets, all socket-specific pins have either A_ or B_ prepended to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.

[2] When a socket is configured as an ATA drive interface, socket interface pin functions change. See Chapter 12.

Table 2-3. Power Control and General Interface Pins

Pin Name	Description	Pin Number		Qty.	I/O	Pwr.	Drive
		Socket A	Socket B				
VPP_VCC	This active-high output controls the socket V_{CC} supply to the socket's $V_{PP}1$ and $V_{PP}2$ pins. The active-high level of this output is mutually exclusive with that of VPP_PGM.	128	135	1	O	1	12 mA
VPP_PGM	This active-high output controls the programming voltage supply to the socket's $V_{PP}1$ and $V_{PP}2$ pins. The active-high level of this output is mutually exclusive with that of VPP_VCC.	127	134	1	O	1	12 mA
-VCC_3	This active-low output controls the 3.3-volt supply to the socket's V_{CC} pins. The active-low level of this output is mutually exclusive with that of -VCC_5.	129	136	1	O	1	12 mA
-VCC_5	This active-low output controls the 5-volt supply to the socket's V_{CC} pins. The active-low level of this output is mutually exclusive with that of -VCC_3.	130	138	1	O	1	12 mA
SPKR_OUT*	**Speaker Output:** This output can be used as a digital output to a speaker to allow a system to support PCMCIA card fax/modem/voice and audio sound output. This output is enabled by setting the socket's **Misc Control 1** register bit 4 to a '1' (for the socket whose speaker signal is to be directed from BVD2/-SPKR/-LED to this pin).	132		1	TO-PU	4	12 mA
LED_OUT*	**LED Output:** This output can be used as an LED driver to indicate disk activity when a socket's BVD2/-SPKR/-LED pin has been programmed for LED support. The **Extension Control 1** register bit 2 must be set to a '1' to enable this output as an LED indicator for the CL-PD6729, and (a) a socket's **ATA Control** register bit 1 must be set to a '1' to allow the level of the particular socket's BVD2/-SPKR/-LED pin to pass through to the LED_OUT* pin, or (b) a socket's **Extension Control 1** bit 1 must be set to a '1' to allow card-cycle activity to cause the LED_OUT* pin to go active low.	133		1	O	4	12 mA

Table 2-4. Power, Ground, and No-Connect Pins

Pin Name	Description	Pin Number	Qty.	I/O	Pwr.	Drive
+5V	This pin is connected to the system's 5-volt power supply, unless 5 volts is not available. In systems where 5 volts is not available, this pin is connected to the system's 3.3-volt supply.	131	1	PW	–	–
CORE_VDD	This pin provides power to the core circuitry of the CL-PD6729. It can be connected to either a 3.3- or 5-volt power supply, independent of the operating voltage of other interfaces. For power conservation on a system with a 3.3-volt supply available, this pin should be connected to the 3.3-volt supply even if there is no intention of operating other interfaces on the device at less than 5 volts.	139	1	PW	–	–
CORE_GND	All CL-PD6729 ground lines should be connected to system ground.	26	1	PW	–	–
RING_GND	All CL-PD6729 ground lines should be connected to system ground.	14, 28, 44, 56, 91, 137, 177	7	PW	–	–
NC	These pins are reserved for future expansion and can be left unconnected. Pin 2 is an output, and pins 3 and 208 are inputs. There is no need to tie input pins 3 and 208 to V_{DD} or ground.	2, 3, 208	3	–	–	–

Table 2-5. Pin Usage Summary

Pin Group	Pin Quantity
PCI bus interface pins	63
Socket interface pins	122
Power control and general interface pins	10
Power, ground, and no-connect pins	13
Total:	208

3. INTRODUCTION TO THE CL-PD6729

3.1 System Architecture

This section describes PCMCIA basics, windowing, socket power management features, interrupts, device power management, write FIFO usage, bus sizing, programmable PCMCIA timing, and ATA mode operation.

3.1.1 PCMCIA Basics

PCMCIA is an abbreviation for Personal Computer Memory Card International Association. PCMCIA 2.1[1] is a standard for using memory and I/O devices as insertable, exchangeable peripherals for PCs (personal computers) and handheld computers.

For simpler end-user and vendor implementation of the standard, systems employing PCMCIA 2.1 should also be backward-compatible with industry-standard PC addressing.

For PCMCIA memory-type cards, the memory information must be mapped into the system memory address space. This is accomplished with a 'windowing' technique that is similar to expanded memory schemes already used in PC systems (for example, LIM 4.0 memory manager).

PCMCIA cards can have *attribute* and *common* memory. Attribute memory is used to indicate to host software the capabilities of the PCMCIA card, and it allows host software to change the configuration of the card. Common memory can be used by host software for any purpose (such as flash file system, system memory, and floppy emulation).

PCMCIA I/O-type cards, such as modems, should also be directly addressable, as if the cards were I/O devices plugged into the PCI bus. For example, it would be highly desirable to have a PCMCIA modem accessible to standard communications software as if it were at a COM port. For COM1, this would require that the modem be accessed at system I/O address 3F8h–3FFh. The method of mapping a PCMCIA I/O address into anticipated areas of PCI I/O space is done similarly to memory windowing.

PCMCIA I/O-type cards usually have interrupts that need to be serviced by host software. For the example of a modem card accessed as if at COM1, software would expect the modem to generate interrupts on the IRQ4 line. To be sure all interrupts are routed as expected, the CL-PD6729 can steer the interrupt from the PCMCIA card to one of the four PCI-bus-defined interrupts or to one of several standard PC interrupts (see Section 3.1.4 and the **Interrupt and General Control** register).

3.1.2 CL-PD6729 Windowing Capabilities

For full compatibility with existing software, and to ensure compatibility with future memory cards and software, the CL-PD6729 provides five programmable memory windows per socket and two programmable I/O windows per socket. These windows can be used by an inserted PCMCIA card to access PCI memory and I/O space.

Having five memory windows per socket allows a memory-type card to be accessed through four memory windows programmed for common memory access, (allowing PC-type expanded-memory-style management), leaving the fifth memory window available to be programmed to access the card's attribute memory without disrupting the common memory in use.

[1] The CL-PD6729 is backward-compatible with PCMCIA standards 1.0, 2.0, and 2.01. The CL-PD6729 is also compatible with JEIDA 4.1 and its earlier standards corresponding with the PCMCIA standards above.

Each memory window has several programming options, including:

Memory Window Option	Description
Enable	Each of the five memory windows can be individually enabled. Disabled windows are not responded to.
Start Address	This is the start address of the memory window within the selected 16-Mbyte page of PCI memory. The start address can be programmed to reside on any 4-Kbyte boundary within the programmed page of PCI memory.
End Address	This is the end address of the memory window within the selected 16-Mbyte page of PCI memory. The end address can be programmed to reside on any 4-Kbyte boundary within the programmed page of PCI memory. Only memory accesses between the start and end address are responded to.
Offset Address	The offset address is added to the PCI address to determine the address for accessing the PCMCIA card. This allows the addresses in the PCMCIA address space to be different from the PCI address space.
Upper Address	The upper memory address specifies a 16-Mbyte page of PCI memory.
Timing	The timing of accesses (Setup/Command/Recovery) can be set by either of two timing register sets: Timer Set 0 or Timer Set 1.
Register Access Setting	The -REG pin can be enabled on a per-window basis so that any of the windows can be used for accessing attribute memory.
Write Protect	If the window is programmed to be write-protected, then writes to the memory window are ignored (reads are still performed normally).

Each I/O window also has several programming options, including:

I/O Window Option	Description
Enable	Each of the two I/O windows can be individually enabled.
Start Address	The start address of the window is programmable on single-byte boundaries from 0 to 64 Kbytes.
End Address	The end address of the window is also programmable on single-byte boundaries from 0 to 64 Kbytes.
Offset Address	The offset address is added to the PCI address to determine the address for accessing the PCMCIA card.
Auto Size	The size of accesses can be set automatically, based on the PCMCIA -IOIS16 signal.
Data Size	The size of accesses can be set manually to either 8 or 16 bits, overriding the Auto Size option.
Timing	The timing of accesses (Setup/Command/Recovery) can be set by either of two timing register sets: Timer Set 0 or Timer Set 1.

CAUTION: The windows of the CL-PD6729 should never be allowed to overlap with each other or the other devices in the system. This would cause signal collisions, resulting in erratic behavior.

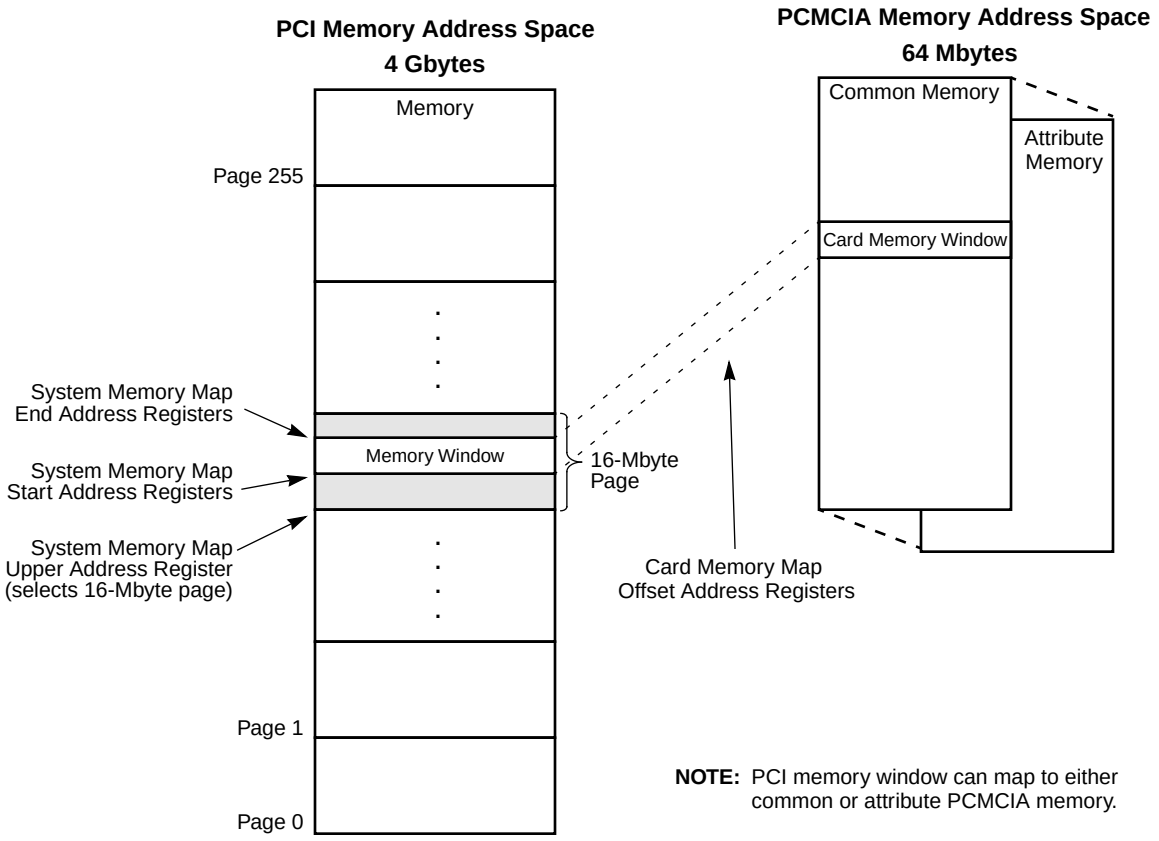


Figure 3-1. Memory Window Organization

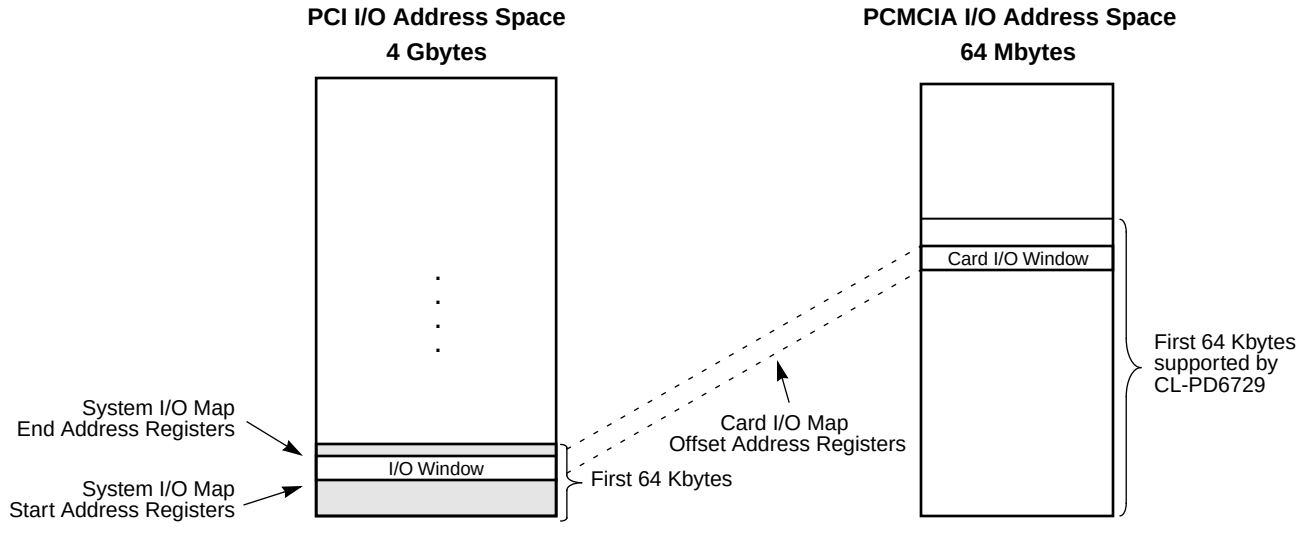


Figure 3-2. I/O Window Organization

3.1.3 Zoomed Video Port

The CL-PD6729 supports the implementation of the ZV (Zoomed Video) Port at the PC Card interface. The ZV Port provides a direct connection between a PC Card and VGA controller and an audio DAC. It allows the PC Card to directly write video data to an input port of a graphics controller and audio data to a digital-to-analog converter.

The CL-PD6729 supports the ZV Port in the "bypass" mode during which the signals are directly routed from the PC Card bus to the video port of the VGA controller. Rerouting is accomplished by tristating address lines A[25:4] from the CL-PD6729. The CL-PD6729 enters the ZV Port mode when the Multimedia Enable bit (bit 0 of the **Misc. Control 1** register at index 16h) and the Multimedia Arm bit (bit 7 of the **Misc. Control 3** register at extended index 25h) are set to a '1'.

Figure 3-3 shows an example of the ZV Port implementation using the CL-PD6729. For more details, refer to the application note *Zoomed Video (ZV) Port Implementation (AN-PD10).*

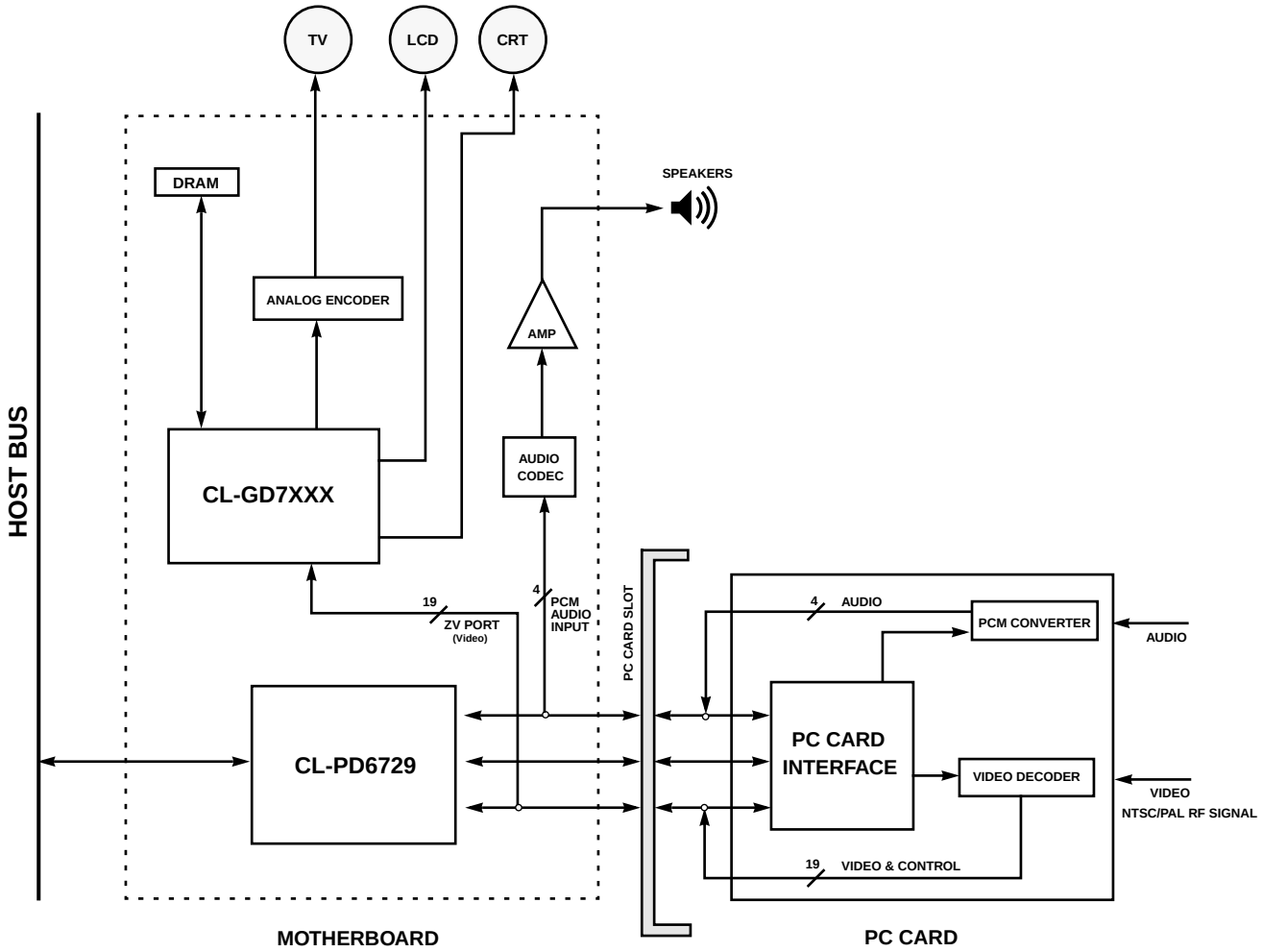


Figure 3-3. A Typical ZV Port Implementation

3.1.4 Interrupts

In a PC-compatible system with a PCI bus, there usually are two types of interrupts in use:

- Four PCI-defined, active-low, open-drain, shared interrupt lines INTA# through INTD#
- A number of ISA-architecture-defined, active-high, totem-pole IRQ output interrupts

The CL-PD6729 provides ten interrupt pins that are individually programmable to work as either PCI-type 'INT#' open-drain interrupts or ISA-type 'IRQ' totem-pole output interrupts. Bits 3 and 4 of the **Extension Control 1** register select PCI-bus or ISA-architecture-compatible interrupt programming.

The CL-PD6729 interrupt pins are labeled with names suggesting their mapping in a PCI-bus-based, ISA-architecture-compatible system, though there are no hard requirements specifying the exact mapping. Typically, all ten interrupt pins should be connected to system interrupt signals to allow maximum flexibility in programming interrupt routing from the CL-PD6729.

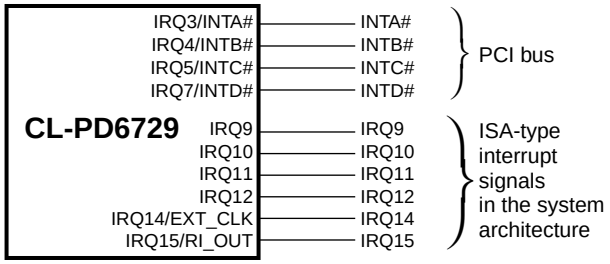


Figure 3-4. A Common Mapping of CL-PD6729 Interrupt Pins to System Interrupt Signals

3.1.4.1 Classes of Interrupts

The CL-PD6729 supports two classes of interrupts:

- Socket or card interrupts initiated by a PCMCIA I/O-type card activating its RDY/-IREQ signal
- Management interrupts triggered by changes in PCMCIA card status

There are four card-status-change conditions that can be programmed to cause management interrupts:

- Card insertion or removal
- Battery warning indicator (BVD2) change on a memory-type card
- Battery dead indicator (BVD1) or I/O-type card status change (STSCHG)
- Ready (RDY) status change on a PCMCIA memory-type card

Either class of interrupts can be routed to any of the ten interrupt pins on the CL-PD6729.

3.1.4.2 Connection of Interrupt Pins Programmed as PCI-Bus INT# Signals

Pins programmed as INT#-type interrupts can be connected to the correspondingly named signals on the PCI bus.

If the management interrupt is being routed to a pin connected to a PCI-bus INT# signal, bit 4 of the **Extension Control 1** register should be set to a '1'. If the card interrupt is being routed to a pin connected to a PCI-bus INT# signal, bit 3 of the **Extension Control 1** register should be set to a '1'.

Although four of the ten CL-PD6729 interrupt pins are labeled as INTA# through INTD#, any of the ten interrupt pins can be used as PCI-type INT# signals.

3.1.4.3 Connection of Interrupt Pins Programmed as ISA-Architecture-Compatible IRQ Signals

IRQ-type interrupts in PC-compatible systems are not generally shared by hardware. Therefore, each device in the system using IRQ-type interrupts must have a unique interrupt line. Additionally, many software applications assume that certain I/O devices use specific IRQ signals. To allow PCMCIA cards with differing I/O functionalities to be connected to appropriate non-conflicting IRQ locations, the CL-PD6729 can steer the interrupt signal from a PCMCIA card to any one of the ten different hardware interrupt lines.

For some I/O-type cards, software is written so that IRQ interrupts can be shared. The CL-PD6729 contains unique logic that allows IRQ-type interrupts to be shared under software control. This is accomplished by programming the CL-PD6729 to alternately pulse and then three-state the desired interrupt pin, which has been programmed as an IRQ-type output. This unique IRQ interrupt sharing technique can be controlled through software so that systems incapable of IRQ sharing have no loss of functionality.

3.1.4.4 Alternate Functions of Interrupt Pins

The CL-PD6729 has two dual-function interrupt pins: IRQ14/EXT_CLK and IRQ15/RI_OUT*. In their default modes, these pins indicate interrupt requests IRQ14 and IRQ15.

IRQ14/EXT_CLK can alternately be configured as an external clock input (EXT_CLK). When configured in External Clock mode by programming **Misc Control 2** register bit 0 to a '1', IRQ14/EXT_CLK acts as a clock input, bringing in an external clock that drives the CL-PD6729 circuitry whenever the PCI bus is inactive.

Similarly, IRQ15/RI_OUT* can alternately be configured to function as a ring indicator output (RI_OUT*) to an 80360-type chip set's -RI input. When configured in Ring Indicate mode by programming **Misc Control 2** register bit 7 to a '1', outputs from a PCMCIA I/O card's -STSCHG pin[1] are passed through to the IRQ15/RI_OUT* pin of the CL-PD6729.

[1] **Interrupt and General Control** register bits 5 and 7 must be set to '1's for a socket interface to accept an -RI input.

3.1.5 CL-PD6729 Power Management

To provide the longest possible battery life, the CL-PD6729 provides many power management features, including Low-power Dynamic mode, Suspend mode, and control of PCMCIA socket power.

Low-power Dynamic mode is transparent to the PCI bus. After reset, the CL-PD6729 is configured for Low-power Dynamic mode. This mode can be turned off by setting **Misc Control 2** register, bit 1 to a '0'. When in Low-power Dynamic mode, periods of inactivity (no activity on the PCMCIA bus and system accesses to chip registers or inserted cards are no longer being performed) cause the CL-PD6729 to enter a low-power state where the clock is turned off to most of the chip and the PCMCIA address and data lines are set to a static value. V_{CC} and V_{PP} power to the card is left unchanged. When there is activity present on the PCMCIA bus, or the system accesses CL-PD6729 registers, or PCMCIA cards are inserted or removed from the socket, the CL-PD6729 enters its active state, services the transaction, and then returns to its low-power state.

A Suspend mode can also be programmed. The CL-PD6729 Suspend mode is the chip's lowest power mode. The CL-PD6729 is put into Suspend mode by setting the **Misc Control 2** register, bit 2 to a '1'. In Suspend mode, all the internal clocks are turned off, and only read/write access to the PCI-Configuration registers, read/write access of the **Index** register, and write access to the **Misc Control 2** register is supported. All accesses to the PCMCIA cards are ignored when in Suspend mode. V_{CC} and V_{PP} power to the card is left unchanged (the system power management software is responsible for turning off power to the socket and entering Suspend mode). Interrupts are passed through to the processor when in Suspend mode. To exit Suspend mode, the **Misc Control 2** register bit 2 must be reset to a '0'.

The CL-PD6729 power can be further managed by controlling socket power as outlined in Section 3.1.6. Socket power can be turned on and off through software or automatically when cards are inserted or removed. The CL-PD6729 provides six pins per socket for controlling external logic to switch V_{CC} and V_{PP} voltages on and off and for sensing a card's operating voltage range. Cards can be turned off when they are not in use.

Table 3-1. CL-PD6729 Power-Management Modes

Mode Name	RST# Level	Misc Control 2 Register		Functionality	Typical Power Consumption (PCI_VCC = 5.0V, PCI_CLK = 33 MHz, CORE_VDD = 3.3V, +5V = 5.0V)
		Suspend Mode (Bit 2)	Low-Power Dynamic Mode (Bit 1)		
Low-power Dynamic (default)	High	0	1	Full functionality	6.4 mW
Normal	High	0	0	Full functionality	14 mW
Suspend (software-controlled)	High	1	–	8-bit access to Misc Control 2 register. No other register access. No card in socket(s).	6.4 mW
Reset	Low	–	–	No register access. No card in socket(s). System bus signals disabled.	21 mW

3.1.6 Socket Power Management Features

Card Removal

When a card is removed from a socket, the CL-PD6729 by default automatically disables the V_{CC} and V_{PP} supplies to the socket. If **Extension Control 1** register bit 1 is a '1', **Power Control** register bit 4 is prevented from being automatically cleared when a card is removed. The CL-PD6729 can also be configured to have management interrupts notify software of card removal.

Card Insertion

At reset, and whenever there is no card in a socket, power to the socket is off. When a card is detected (card detect input pins, -CD1 and -CD2, to the CL-PD6729 become asserted low), two independent actions can be programmed to occur.

If the CL-PD6729 has been set for automatic power-on (**Power Control** register bits 4 and 5 are both '1's), the CL-PD6729 automatically enables the socket V_{CC} supply (and, if so programmed, V_{PP} supply).

If the CL-PD6729 has been programmed to cause management interrupts for card-detection events, assertion of -CD1 and -CD2 to the CL-PD6729 causes a management interrupt to be generated to inform system software that a card was inserted. In the case of manual power detection (**Power Control** register bits 5 is a '0'), system software can then determine the card's operating voltage range and then power-up the socket and initialize the card, or if programmed for automatic power-on (**Power Control** register bits 5 is a '1' and **Extension Control 1** register bit 1 is a '1'), simply initialize the card.

3.1.7 Write FIFO

To increase performance when writing to PCMCIA cards, two, independent, four-word-deep write FIFOs are used. Writes to PCMCIA cards will complete without holding off the PCI bus until the FIFO is full.

NOTE: Register states should only be changed when the write FIFO is empty.

3.1.8 Bus Sizing

The CL-PD6729 operates in 32-bit mode. All PCI transactions are 32-bit, even when supporting 8-bit-only or 16-bit PCMCIA cards.

3.1.9 Programmable PCMCIA Timing

The Setup, Command, and Recovery time for the PCMCIA bus is programmable (see Chapter 11). The CL-PD6729 can be programmed to match the timing requirements of any PCMCIA card. There are two sets of timing registers, Timer Set 0 and Timer Set 1, that can be selected on a per-window basis for both I/O and memory windows.

By setting one of the timing sets for a Recovery time equal to flash memory programming time and utilizing the write FIFO, algorithms can be created to relieve system software of the necessity of doing timing loops, and thus allow for flash programming in the background.

3.1.10 ATA Mode Operation

The CL-PD6729 supports direct connection to AT-attached-interface hard drives. ATA drives use an interface very similar to the IDE interface found on many popular portable computers. See Chapter 12 for more information.

3.1.11 VS1 and VS2

The pins VS1 and VS2 can be used to determine the voltage capabilities of an inserted card. The status of these pins, for both sockets, are indicated by bits 3:0 of the **External Data** register at extended index 0Ah of index 6Fh (this is true even though registers 40h–7Fh are generally for Socket B only).

3.2 Host Access to Registers

The CL-PD6729 registers are accessed through an 8-bit indexing mechanism. An index register scheme allows a large number of internal registers to be accessed by the CPU using only two I/O addresses.

The **Index** register (see Chapter 6) is used to specify which of the internal registers the CPU will access next. The value in the **Index** register is called the Register Index and is the number that specifies a unique internal register. The **Data** register is used by the CPU to read and write the internal register specified by the **Index** register.

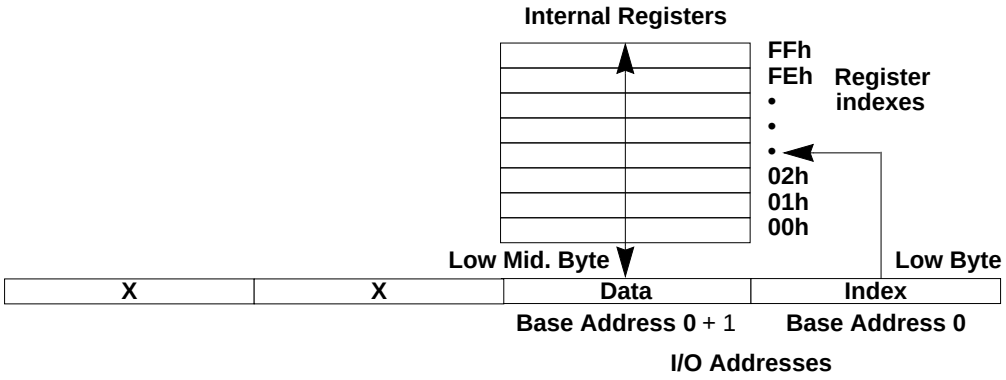


Figure 3-5. Indexed 8-Bit Register Structure

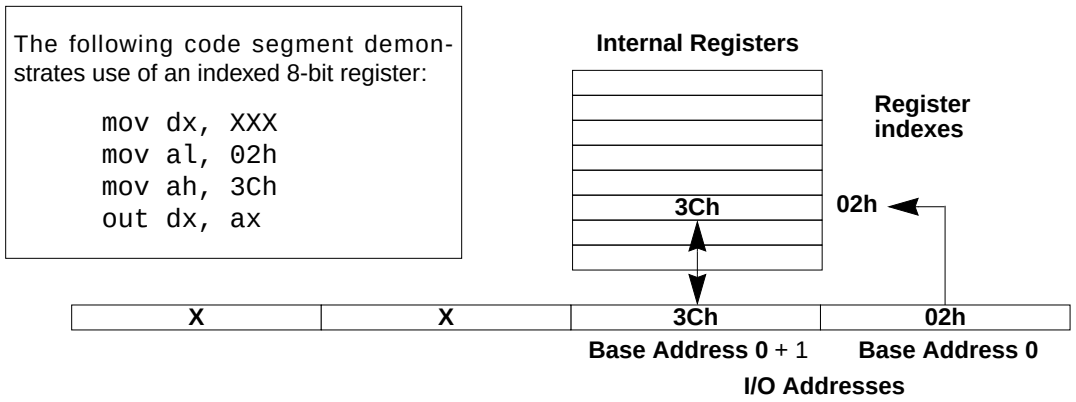


Figure 3-6. Indexed 8-Bit Register Example

The CL-PD6729 has Extension registers that add to the functionality of the 82365SL-compatible register set. Within the Extension registers is an **Extended Index** register and **Extended Data** register that provide access to more registers. The registers accessed through **Extended Index** and **Extended Data** are thus double indexed. The example below shows how to access the **Extension Control 1** register, one of the double-indexed registers.

```
;Write to Extension Control 1 register example

;Constants section
   Extended_Index     EQU 2Eh
   Index_Reg          EQU 2Fh
   Ext_Cntrl_1        EQU 03h
   Base_IO_Address    EQU XXX
      ;The base I/O address for the CL-PD6729
      ;should be obtained through PCI BIOS.

;Code section
   mov   dx, Base_IO_Address
   mov   al, Extended_Index
   mov   ah, Ext_Cntrl_1
   out   dx, ax
   mov   al, Index_Reg
   mov   ah, user_data          ;Desired data to be
   out   dx, ax                 ;written to
                                ;extended index 3

;Read from Extension Control 1 register example

;Code section
   mov   dx, Base_IO_Address
   mov   al, Extended_Index
   mov   ah, Ext_Cntrl_1
   out   dx, ax
   mov   al, Index_Reg
   out   dx, al
   inc   dx                     ;al has extended
   in    al, dx                 ;index 3 data
```

3.3 Power-On Setup

Following RST#-activated reset, the CL-PD6729 must be configured by host initialization or BIOS software. The application of the RST# signal on power-up causes initialization of all the CL-PD6729 register bits and fields to their reset values.

4. REGISTER DESCRIPTION CONVENTIONS

Register Headings

The description of each register starts with a header containing the following information:

Header Field	Description
Register Name	This indicates the register name.
Offset	This is added to the base address to generate the total effective address. This field is for PCI-Configuration registers only.
Register Per	This indicates whether the register affects both sockets, marked *chip*, or an individual socket, marked *socket*. If *socket* is indicated, there are two registers being described, each with a separate Index value (one for each socket, A and B). [a]
Index [a]	This is the Index value through which an internal register in an indexed register set is accessed.
Register Compatibility Type	This indicates whether the register is 82365SL-compatible, marked *365* or a register extension, marked *ext*.

[a] When the register is socket-specific, the Index value given in the register heading is for Socket A only. For the Socket B register, add 40h to the Index value of the Socket A register.

Special Function Bits

Following is a description of bits with special functions:

Bit Type	Description
Reserved	These bits are Reserved and should not be changed.
Compatibility Bit	These bits have no function on the CL-PD6729 but are included for compatibility with the 82365SL register set.
0 or *1*	These read-only bits are forced to either a '0' or '1' at reset and cannot be changed.
Scratchpad Bit	These read/write bits are available for use as bits of memory.

Bit Naming Conventions

The following keywords are used within bit and field names:

Keyword	Description
Enable	Indicates that the function described in the rest of the bit name is active when the bit is a '1'.
Disable	Indicates that the function described in the rest of the bit name is active when the bit is a '0'.
Mode	Indicates that the function of the bit alters the interpretation of the values in other registers.
Input	Indicates a bit or field that is read from a pin.
Output	Indicates a bit or field that is driven to a pin.
Select	Indicates that the bit or field selects between multiple alternatives. Fields that contain *Select* in their names have an indirect mapping between the value of the field and the effect.
Status	Indicates one of two types of bits: either Read-only bits used by the CL-PD6729 to report information to the system or bits set by the CL-PD6729 in response to an event, and can also be cleared by the system. The system cannot directly cause a Status bit to become a '1'.
Value	Indicates that the bit or field value is used as a number.

Bit Descriptions

When used to describe an action taken by the host system, the phrase "the system *sets* a bit" is the same as stating "the system writes the appropriate register with a '1' (one) in the bit".

Similarly, the phrase "the system *resets* a bit" or "the system *clears* a bit" is the same as stating "the system writes the appropriate register with a '0' (zero) in the bit".

5. PCI-CONFIGURATION REGISTERS

These registers occupy offsets 00–3Fh. They control basic PCI bus functionality. PCMCIA Operation registers are accessed through the **Base Address 0** register. The registers in this section apply to the entire chip; they are not specific to either socket.

CAUTION: If bits indicated as read only (R:) are to be written to, they should be written to a '0'.

5.1 Vendor ID and Device ID

Configuration Register Name: **Vendor ID and Device ID**
Offset: **00h** *Register Per:* chip

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Byte 3 **Device ID** *(high)*	Device ID *(high)* R:00010001							
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Byte 2 **Device ID** *(low)*	Device ID *(low)* R:00000000							
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Byte 1 **Vendor ID** *(high)*	Vendor ID *(high)* R:00010000							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0 **Vendor ID** *(low)*	Vendor ID *(low)* R:00010011							

Bits 15-0: Vendor ID

This read-only field is the vendor identification assigned to Cirrus Logic by the PCI Special Interest Group. This field always reads back 1013h.

Bits 31-16: Device ID

This read-only field is the device identification assigned to this device by Cirrus Logic. This field always reads back 1100h for the CL-PD6729. (Revision number identification for the CL-PD6729 part itself is indicated by the Mask Revision byte at extended index 34h.

5.2 Command and Status

Configuration Register Name: **Command and Status**
Offset: **04h** *Register Per:* chip

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Byte 3 **Status** *(high)*	Address/Data Parity Error Detected	System Error (SERR#) Generated	*Reserved*			DEVSEL# Timing		Master Data Parity Error Reported
	RW:0	RW:0	R:XXX			R:10		R:0
	Bit 23	*Bit 22*	*Bit 21*	*Bit 20*	*Bit 19*	*Bit 18*	*Bit 17*	*Bit 16*
Byte 2 **Status** *(low)*	*Reserved* R:XXXXXXXX							
	Bit 15	*Bit 14*	*Bit 13*	*Bit 12*	*Bit 11*	*Bit 10*	*Bit 9*	*Bit 8*
Byte 1 **Command** *(high)*	*Reserved* R:XXXXXXX							System Error (SERR#) Enable RW:0
	Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Byte 0 **Command** *(low)*	Wait Cycle Enable	Parity Error Check/Report Enable	*Reserved*				PCI Memory Space Enable	PCI I/O Space Enable
	R:1	RW:0	R:XXXX				RW:0	RW:0

Bit 0: PCI I/O Space Enable

0	The I/O space for the CL-PD6729 is disabled. Any reads or writes to the I/O space will be ignored. This applies to both the I/O registers of the CL-PD6729 itself, as well as any I/O windows that might have been enabled to the PCMCIA sockets.
1	The I/O space for the CL-PD6729 is enabled and will respond to reads and writes to the I/O address range defined in **Base Address 0** register as well as any I/O window addresses.

Bit 1: PCI Memory Space Enable

This bit must be set or the CL-PD6729 will not respond to memory transactions.

0	The memory space for the CL-PD6729 is disabled. Any reads or writes to the CL-PD6729 memory space will be ignored.
1	The memory space for the CL-PD6729 is enabled, allowing memory window access.

Bit 6: Parity Error Check/Report Enable

This bit enables all parity-reporting-related circuitry, except for bit 31 of this register.

0	Parity checking and reporting in the CL-PD6729 disabled.
1	Parity checking and reporting in the CL-PD6729 is enabled.

Bit 7: Wait Cycle Enable

This bit always reads a ‘1’, indicating that the CL-PD6729 employs address stepping.

Bit 8: System Error (SERR#) Enable

This bit enables the CL-PD6729's reporting of system errors by assertion of the SERR# pin when address parity errors occur. Bit 6 must also be set to a '1' to allow detecting of conditions that allow SERR# activation. See also description of bit 30.

0	Activation of SERR# on address parity error is disabled.
1	SERR# is activated whenever an address parity error is internally detected (slave mode).

Bit 24: Master Data Parity Error Reported

This bit is Reserved and will always read a '0'.

Bits 26-25: DEVSEL# Timing

This field always reads back '10', identifying the CL-PD6729 as a slow-speed device.

Bits 29-27: Reserved

These bits are reserved for future use. On writes to this register, these bits should be written as '0'. The value of these bits should be considered as indeterminate on reads of this register.

Bit 30: System Error (SERR#) Generated

This bit is set whenever the CL-PD6729 asserts SERR# because of internal detection of a PCI address parity error. Bit 8 of this register must be set before system errors can be reported, and bit 6 must be set to allow address parity errors to be detected. The CL-PD6729 only asserts SERR# if address parity errors occur. No other chip or system actions will cause SERR# to be driven active.

0	SERR# was not asserted by this device.
1	SERR# was asserted by this device, indicating a PCI address parity error.

Bit 31: Address/Data Parity Error Detected

This bit indicates whether a parity error was detected, independently of whether bit 6 of this register is a '1'.

0	No data parity errors detected.
1	Address or data parity error detected.

5.3 Revision ID and Class Code

Configuration Register Name: **Revision ID and Class Code**
Offset: **08h** *Register Per:* chip

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Byte 3 **Class Code** *(high)*	Class Code *(high)* R:00000110							
	Bit 23	*Bit 22*	*Bit 21*	*Bit 20*	*Bit 19*	*Bit 18*	*Bit 17*	*Bit 16*
Byte 2 **Class Code** *(mid.)*	Class Code *(mid.)* R:00000101							
	Bit 15	*Bit 14*	*Bit 13*	*Bit 12*	*Bit 11*	*Bit 10*	*Bit 9*	*Bit 8*
Byte 1 **Class Code** *(low)*	Class Code *(low)* R:00000000							
	Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Byte 0 **Revision ID**	Revision ID R:nnnnnnnn[a]							

[a] This read-only value depends on the revision level of the CL-PD6729. For CL-PD6729 Revision E or later, these bits correspond to the value of the Mask Revision Byte register at extended index 34h.

Bits 7-0: Revision ID

This read-only field identifies the revision level of the CL-PD6729 chip.

Bits 31-8: Class Code

This field always reads back 060500h, identifying the CL-PD6729 as a PCI-to-PCMCIA bridge device.

5.4 Cache Line Size, Latency Timer, Header Type, and BIST

Configuration Register Name: **Cache Line Size, Latency Timer, Header Type, and BIST**

Offset: **0Ch** *Register Per:* chip

	Bit 31	*Bit 30*	*Bit 29*	*Bit 28*	*Bit 27*	*Bit 26*	*Bit 25*	*Bit 24*
Byte 3 **BIST**	*Reserved* R:XXXXXXXX							
	Bit 23	*Bit 22*	*Bit 21*	*Bit 20*	*Bit 19*	*Bit 18*	*Bit 17*	*Bit 16*
Byte 2 **Header Type**	Header Type R:00000000							
	Bit 15	*Bit 14*	*Bit 13*	*Bit 12*	*Bit 11*	*Bit 10*	*Bit 9*	*Bit 8*
Byte 1 **Latency Timer**	*Reserved* R:XXXXXXXX							
	Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Byte 0 **Cache Line Size**	*Reserved* R:XXXXXXXX							

Bits 31:24 BIST Register

These bits will always read back 00h. The CL-PD6729 uses proprietary manufacturing test methods instead of BIST test features.

Bits 23:16 Header Type Register

These bits will always read back 00h and specifies that the CL-PD6729 uses the standard type 00 configuration space header register layout for configuration bytes 10h through 3Fh.

Bits 31:24 Latency Timer Register

Since the CL-PD6729 does not use bus mastering, this bit field is always 00h.

Bits 7:0 Cache Line Size

These bits will always read back 00h, indicating that the CL-PD6729 does not participate in PCI-defined caching algorithms.

5.5 Base Address 0

Configuration Register Name: **Base Address 0**
Offset: **10h** *Register Per:* chip

	Bit 31	*Bit 30*	*Bit 29*	*Bit 28*	*Bit 27*	*Bit 26*	*Bit 25*	*Bit 24*
Byte 3	I/O Base Address *(high)* RW:00000000							
	Bit 23	*Bit 22*	*Bit 21*	*Bit 20*	*Bit 19*	*Bit 18*	*Bit 17*	*Bit 16*
Byte 2	I/O Base Address *(high mid.)* RW:00000000							
	Bit 15	*Bit 14*	*Bit 13*	*Bit 12*	*Bit 11*	*Bit 10*	*Bit 9*	*Bit 8*
Byte 1	I/O Base Address *(low mid.)* RW:00000000							
	Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Byte 0	I/O Base Address *(low)* RW:000000						*Reserved* R:0	I/O Space Indicator R:1

This is the PCI I/O address space base address for the Operation registers.

Bit 0: I/O Space Indicator

This bit always reads back a ‘1’, indicating that this base address register defines a PCI I/O space.

Bit 1: Reserved

This bit is a read-only ‘0’ in accordance with the PCI specification for I/O base address configuration registers.

Bits 31-2: I/O Base Address

This bit is a read-only ‘0’ in accordance with the PCI specification for I/O base address configuration registers.

5.6 Interrupt Line, Interrupt Pin, Min_Gnt, and Max_Lat

Configuration Register Name: **Interrupt Line, Interrupt Pin, Min_Gnt, and Max_Lat**
Offset: **3Ch** *Register Per:* chip

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Byte 3 **Max_Lat**	Max_Lat R:00000000							
	Bit 23	*Bit 22*	*Bit 21*	*Bit 20*	*Bit 19*	*Bit 18*	*Bit 17*	*Bit 16*
Byte 2 **Min_Gnt**	*Reserved* R:XXXXXXXX							
	Bit 15	*Bit 14*	*Bit 13*	*Bit 12*	*Bit 11*	*Bit 10*	*Bit 9*	*Bit 8*
Byte 1 **Interrupt Pin**	Interrupt Pin R:00000001							
	Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Byte 0 **Interrupt Line**	Interrupt Line RW:00000000							

Bits 7-0: Interrupt Line

For other than PCMCIA-controller-type PCI devices, this field indicates interrupt line routing. Although this register is read/write for PCI compatibility, no interrupt line routing is controlled by this register on the CL-PD6729. Because the CL-PD6729 must dynamically configure interrupt usage, the actual routing to the appropriate interrupt line is made by writing to interrupt-type-specific interrupt control bit settings in the Operation registers (see the **Interrupt and General Control** register).

Bits 15-8: Interrupt Pin

For other than PCMCIA-controller-type PCI devices, this read-only field indicates which interrupt pin the device uses. Because the CL-PD6729 must dynamically configure interrupt usage, the actual connection of interrupt pins is defined by interrupt control bit settings in the Operation registers (see the **Management Interrupt Configuration** register). This field always reads back 01h.

Bits 31-24: Max_Lat

This field indicates the maximum time that can occur between PCI bus accesses to the CL-PD6729 while still efficiently performing transfers to or from PCMCIA cards. The value programmed is in 250-ns increments, based on full-speed PCI_CLK operation. This field always reads back 00h, indicating that there are no major latency requirements.

6. OPERATION REGISTERS

The CL-PD6729's internal Device Control, Window Mapping, Extension, and Timing registers are accessed through a pair of Operation registers — an **Index** register and a **Data** register.

The **Index** register is accessed at the address programmed in the **Base Address 0** register, and the **Data** register (see page 37) is accessed by adding 1 to the address programmed in **Base Address 0**.

Figure 6-1. Operation Registers as PCI Double-Word I/O Space at Base Address 0 Register (programmed at offset 10h)

6.1 Index

Register Name: **Index** *Register Per:* chip
Index: **n/a** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved	Socket Index	Register Index					
RW:0	RW:0	RW:000000					

Bits 5-0: Register Index

These bits determine which of the 64 possible socket-specific registers will be accessed when the **Data** register is next accessed by the processor. Note that some values of the Register Index field are reserved, see Table 6-1.

Bit 6: Socket Index

This bit determines which set of socket-specific registers is currently selected. When this bit is a '0', a Socket A register is selected; when this bit is a '1', a Socket B register is selected.

The **Index** register value determines which internal register should be accessed (read or written) in response to each CPU access of the **Data** register. Each of the two possible PCMCIA sockets is allocated 64 of the 256 locations in the internal register index space.

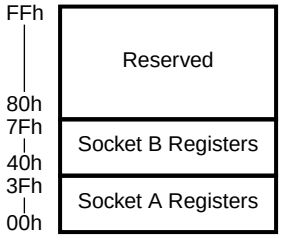


Figure 6-2. Socket/Register Index Space

When viewed as a 7-bit value, the contents of this register completely specify a single internal-register byte. For example, when the value of this register is in the range 00h–3Fh, a Socket A register is selected (Socket Index bit is a '0'), and when the value of this register is in the range 40h–7Fh, a Socket B register is selected (Socket Index bit is a '1').

The internal register that is accessed when the CPU reads or writes the **Data** register is determined by the current value of the **Index** register, as follows:

Table 6-1. Index Registers

Register Name	Index Value		Chapter	Page Number
	Socket A	Socket B		
Chip Revision	00h[a]		Chapter 7: Device Control	38
Interface Status	01h	41h		39
Power Control	02h	42h		41
Interrupt and General Control	03h	43h		43
Card Status Change	04h	44h		45
Management Interrupt Configuration	05h	45h		46
Mapping Enable	06h	46h		48
I/O Window Control	07h	47h	Chapter 8: I/O Window Mapping	50
System I/O Map 0 Start Address Low	08h	48h		51
System I/O Map 0 Start Address High	09h	49h		51
System I/O Map 0 End Address Low	0Ah	4Ah		52
System I/O Map 0 End Address High	0Bh	4Bh		52
System I/O Map 1 Start Address Low	0Ch	4Ch		51
System I/O Map 1 Start Address High	0Dh	4Dh		51
System I/O Map 1 End Address Low	0Eh	4Eh		52
System I/O Map 1 End Address High	0Fh	4Fh		52
System Memory Map 0 Start Address Low	10h	50h	Chapter 9: Memory Window Mapping	54
System Memory Map 0 Start Address High	11h	51h		55
System Memory Map 0 End Address Low	12h	52h		55
System Memory Map 0 End Address High	13h	53h		56
Card Memory Map 0 Offset Address Low	14h	54h		57
Card Memory Map 0 Offset Address High	15h	55h		57
Misc Control 1	16h	56h	Chapter 10: Extension	59
FIFO Control	17h	57h		61
System Memory Map 1 Start Address Low	18h	58h	Chapter 9: Memory Window Mapping	54
System Memory Map 1 Start Address High	19h	59h		55
System Memory Map 1 End Address Low	1Ah	5Ah		55
System Memory Map 1 End Address High	1Bh	5Bh		56
Card Memory Map 1 Offset Address Low	1Ch	5Ch		57
Card Memory Map 1 Offset Address High	1Dh	5Dh		57
Misc Control 2	1Eh[a]		Chapter 10: Extension	62
Chip Information	1Fh[a]			63
System Memory Map 2 Start Address Low	20h	60h	Chapter 9: Memory Window Mapping	54
System Memory Map 2 Start Address High	21h	61h		55
System Memory Map 2 End Address Low	22h	62h		55

Table 6-1. Index Registers *(cont.)*

Register Name	Index Value		Chapter	Page Number
	Socket A	Socket B		
System Memory Map 2 End Address High	23h	63h	Chapter 9: Memory Window Mapping	56
Card Memory Map 2 Offset Address Low	24h	64h		57
Card Memory Map 2 Offset Address High	25h	65h		57
ATA Control	26h	66h	Chapter 10: Extension	64
Scratchpad	27h	67h	–	–
System Memory Map 3 Start Address Low	28h	68h	Chapter 9: Memory Window Mapping	54
System Memory Map 3 Start Address High	29h	69h		55
System Memory Map 3 End Address Low	2Ah	6Ah		55
System Memory Map 3 End Address High	2Bh	6Bh		56
Card Memory Map 3 Offset Address Low	2Ch	6Ch		57
Card Memory Map 3 Offset Address High	2Dh	6Dh		57
Extended Index:	2Eh	6Eh	Chapter 10: Extension	65
Scratchpad	Extended index 00h			–
Reserved	Extended index 01h			–
Reserved	Extended index 02h			–
Extension Control 1	Extended index 03h			66
Reserved	Extended index 04h			–
System Memory Map 0 Upper Address	Extended index 05h			67
System Memory Map 1 Upper Address	Extended index 06h			67
System Memory Map 2 Upper Address	Extended index 07h			67
System Memory Map 3 Upper Address	Extended index 08h			67
System Memory Map 4 Upper Address	Extended index 09h			67
External Data[b]	Extended index 0Ah			73
Misc. Control 3	Extended index 25h			67
Mask Revision Byte[c]	Extended index 34h			68
Product ID Byte[c]	Extended index 35h			69
Device Capability Byte A[c]	Extended index 36h			69
Device Capability Byte B[c]	Extended index 37h			70
Device Implementation Byte A[c]	Extended index 38h			70
Device Implementation Byte B[c]	Extended index 39h			71
Device Implementation Byte C[c]	Extended index 3Ah			72
Device Implementation Byte D[c]	Extended index 3Bh			73
Extended Data	2Fh	6Fh		66
System Memory Map 4 Start Address Low	30h	70h	Chapter 9: Memory Window Mapping	54
System Memory Map 4 Start Address High	31h	71h		55
System Memory Map 4 End Address Low	32h	72h		55
System Memory Map 4 End Address High	33h	73h		56
Card Memory Map 4 Offset Address Low	34h	74h		57
Card Memory Map 4 Offset Address High	35h	75h		57
Card I/O Map 0 Offset Address Low	36h	76h	Chapter 8: I/O Window Mapping	53
Card I/O Map 0 Offset Address High	37h	77h		53
Card I/O Map 1 Offset Address Low	38h	78h		53
Card I/O Map 1 Offset Address High	39h	79h		53

Table 6-1. Index Registers *(cont.)*

Register Name	Index Value		Chapter	Page Number
	Socket A	Socket B		
Setup Timing 0	3Ah	7Ah	Chapter 11: Timing	74
Command Timing 0	3Bh	7Bh		75
Recovery Timing 0	3Ch	7Ch		76
Setup Timing 1	3Dh	7Dh		74
Command Timing 1	3Eh	7Eh		75
Recovery Timing 1	3Fh	7Fh		76
Reserved	80h–FFh		–	–

[a] This register affects both sockets (it is not specific to either socket).

[b] This register is only applicable for the extended index 6F register.

[c] This register is only applicable for the extended index 2F register.

6.2 Data

Register Name: **Data**							*Register Per:* chip
Index: **n/a**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Data							

The **Data** register is accessed at **Base Address 0** + 1. This register indicates the contents of the register at the Socket/Register Index selected by the **Index** register.

7. DEVICE CONTROL REGISTERS

7.1 Chip Revision

Register Name: **Chip Revision** *Register Per:* chip
Index: **00h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Interface ID		*Reserved 0*	*Reserved 0*	Revision			
R:10		R:0	R:0	R:0010[a]			

[a] Value for the current stepping only.

Bits 3-0: Revision

This field indicates the CL-PD6729's compatibility with the 82365SL A-step.

Bits 5-4: Reserved

These bits will always read back as '0'.

Bits 7-6: Interface ID

00	I/O only.
01	Memory only.
10	Memory and I/O.
11	Reserved.

These bits identify what type of interface this controller supports. The CL-PD6729 supports both memory and I/O interface PCMCIA cards.

7.2 Interface Status

Register Name: **Interface Status** *Register Per:* socket
Index: **01h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
		RDY	*WP*	*-CD2*	*-CD1*	*BVD2*	*BVD1*
1	Card Power On	Ready/Busy*	Write Protect	Card Detect		Battery Voltage Detect	
R:1[a]	R:0	R[b]	R[c]	R[d]		R[e]	

[a] Bit 7 always reads a '1' on the CL-PD6729.
[b] Bit 5 indicates the value of the RDY/-IREQ pin (see page 12).
[c] Bit 4 indicates the value of the WP/-IOIS16 pin (see page 12).
[d] Bits 3-2 indicate the inversion of the values of the -CD1 and -CD2 pins (see page 12).
[e] Bits 1-0 indicate the values of the BVD1/-STSCHG/-RI and BVD2/-SPKR/-LED pins (see page 13).

Bits 1-0: Battery Voltage Detect

BVD2 Level	BVD1 Level	Bit 1	Bit 0	PCMCIA Interpretation
Low	Low	0	0	Card data lost
Low	High	0	1	Battery low warning
High	Low	1	0	Card data lost
High	High	1	1	Battery/data okay

In Memory Card Interface mode, these bits are used by PCMCIA support software and firmware to indicate the remaining capacity of the battery in battery-backed cards. In I/O Card Interface mode, bit 0 indicates the state of the BVD1/-STSCHG/-RI pin (see page 13). Bit 1 status is not valid in I/O Card Interface mode.

Bits 3-2: Card Detect

-CD2 Level	-CD1 Level	Bit 3	Bit 2	Card Detect Status
High	High	0	0	Either no card or card is not fully inserted
High	Low	0	1	Card is not fully inserted
Low	High	1	0	Card is not fully inserted
Low	Low	1	1	Card is fully inserted

These bits indicate the state of the -CD1 and -CD2 pins (see page 12).

Bit 4: Write Protect

0	Card is not write protected.
1	Card is write protected.

In Memory Card Interface mode, this bit indicates the state of the WP/-IOIS16 pin (see page 12) on the card. This bit is not valid in I/O Card Interface mode.

Bit 5: Ready/Busy*

0	Card is not ready.
1	Card is ready.

In Memory Card Interface mode, this bit indicates the state of the RDY/-IREQ pin (see page 12) on the card. This status bit is only defined for Memory Card Interface mode and is not valid in I/O Card Interface mode.

Bit 6: Card Power On

0	Power to the card is not on.
1	Power to the card is on.

This status bit indicates whether power to the card is on. Refer to the Table 7–1 for more details.

7.3 Power Control

Register Name: **Power Control** *Register Per:* socket
Index: **02h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Card Enable	*Compatibility Bit*	Auto-Power	V_{CC} Power	*Compatibility Bits*		$V_{PP}1$ Power	
RW:0	RW:0	RW:0	RW:0	RW:00		RW:00	

Table 7–1. Enabling of Socket Power Controls

RST# Level	Both -CD1 and -CD2 are Active (Low)	Power Control Register		Interface Status Register (see page 39)	-VCC_3 and -VCC_5 Levels	VPP_PGM and VPP_VCC Levels
		V_{CC} Power (Bit 4)	Auto-Power (Bit 5)	Card Power On (Bit 6)		
Low	X	X	X	0	Inactive (high)	Inactive (low)
High	X	0	X	0	Inactive (high)	Inactive (low)
High	X	1	0	1	Activated per **Misc Control 1** register, bit 1	Activated per **Power Control** register, bits 1 and 0
High	No	1	1	0	Inactive (high)	Inactive (low)
High	Yes	1	1	1	Activated per **Misc Control 1** register, bit 1	Activated per **Power Control** register, bits 1 and 0

Table 7–2. Enabling of Output Signals to Socket

RST# Level	Both -CD1 and -CD2 are Active (Low)	Power Control Register		CL-PD6729 Output Signals to Socket
		V_{CC} Power (Bit 4)	Card Enable (Bit 7)	
Low	X	X	X	High impedance
High	No	X	X	High impedance
High	Yes	0	0	High impedance
High	Yes	0	1	Enabled
High	Yes	1	0	High impedance
High	Yes	1	1	Enabled

Bits 1-0: $V_{PP}1$ Power

Bit 1	Bit 0	VPP_PGM	VPP_VCC	PCMCIA Intended Socket Function
0	0	Inactive (low)	Inactive (low)	Zero volts to PCMCIA socket $V_{PP}1$ pin
0	1	Inactive (low)	Active (high) [a]	Selected card V_{CC} to PCMCIA socket $V_{PP}1$ pin
1	0	Active (high) [a]	Inactive (low)	+12V to PCMCIA socket $V_{PP}1$ pin
1	1	Inactive (low)	Inactive (low)	Zero volts to PCMCIA socket $V_{PP}1$ pin

[a] Under conditions where $V_{PP}1$ power is activated. See Table 7–1.

These bits control the power to the $V_{PP}1$ pin of the PCMCIA card.

Bit 4: V_{CC} Power

0	Power is not applied to the card: the -VCC_3 and -VCC_5 socket power control pins are inactive (high).
1	Power is applied to the card: if bit 5 is a ‘0’, or bit 5 is a ‘1’ and -CD2 and -CD1 are active low, then the selected -VCC_3 or -VCC_5 socket power control pin is active (low).

Depending on the value of bit 5 below, setting this bit to a ‘1’ applies power to the card. The V_{CC} 3.3V bit (see page 59) determines whether 3.3V or 5V power is applied. Note that this bit is reset to a ‘0’ when a card is removed from the socket unless the auto-power-off feature is disabled by setting **Extension Control 1** register bit 1 to a ‘1’; a write is required to reactivate power to the card.

Extension Control 1 register bit 0, when set to ‘1’, prevents modification of the VCC Power bit by writes to the Power Control register.

Bit 5: Auto-Power

0	V_{CC} and $V_{PP}1$ power control signals are activated independent of the socket’s -CD2 and -CD1 input levels.
1	V_{CC} and $V_{PP}1$ power control signals are only activated if the socket’s -CD2 and -CD1 inputs are both active (low).

When this bit is set to a ‘1’, the CL-PD6729 allows power to the card to be turned on and off automatically with the insertion and removal of a PCMCIA card.

Bit 7: Card Enable

0	Outputs to card socket are not enabled and are floating.
1	Outputs to card socket are enabled if -CD1 and -CD2 are active low and bit 4 is a ‘1’.

When this bit is a ‘1’, the outputs to the PCMCIA card are enabled if a card is present and card power is being supplied. The pins affected include -CE2, -CE1, -IORD, -IOWR, -OE, -REG, RESET, A[25:0], D[15:0], and -WE.

7.4 Interrupt and General Control

Register Name: **Interrupt and General Control** *Index:* **03h**							*Register Per:* socket *Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Ring Indicate Enable	Card Reset*	Card Is I/O	Manage Int Enable	IRQ Level			
RW:0	RW:0	RW:0	RW:0	RW:0000			

Bits 3-0: IRQ Level

0000	IRQ disabled
0001	Reserved
0010	Reserved
0011	IRQ3 (INTA#)
0100	IRQ4 (INTB#)
0101	IRQ5 (INTC#)
0110	Reserved
0111	IRQ7 (INTD#)
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14 (This output can alternately be used as external clock input.)
1111	IRQ15 (This output can alternately be used as ring indicate output.)

These bits determine which IRQ will occur when the card causes an interrupt through the RDY/-IREQ pin on the PCMCIA socket.

Bit 4: Manage Int Enable

0	Management IRQ (see page 47) specifies management interrupt bits.
1	Reserved. No hardware function in the CL-PD6729.

This bit was created to determine how management interrupts occur on ISA-based systems. It is included for software compatibility. Because there is no -INTR pin on the PCI bus, setting this bit to a '1' would cause management interrupts not to occur.

Bit 5: Card Is I/O

0	Sets Memory Card Interface mode. The card socket is configured to support memory-only-type cards. All dual-function socket interface pins are defined to perform memory-only-type interface functions.
1	Sets I/O Card Interface mode. The card socket is configured to support combined I/O-and-memory-type cards. All dual-function socket interface pins are defined to perform all I/O and basic memory type interface functions.

This bit determines how dual-function socket interface pins will be used. For more information on specific pins, refer to Table 2-2 in Chapter 2.

Bit 6: Card Reset*

0	The RESET signal to the card socket is set active (high for normal, low for ATA mode).
1	The RESET signal to the card socket is set inactive (low for normal, high for ATA mode).

This bit determines whether the RESET signal (see page 12) to the card is active or inactive. When the Card Enable bit (see page 42) is a '0', the RESET signal to the card is high impedance. See Chapter 12 for further description of ATA mode functions.

Bit 7: Ring Indicate Enable

0	BVD1/-STSCHG/-RI pin is status change function.
1	BVD1/-STSCHG/-RI pin is ring indicate input pin from card.

In I/O Card Interface mode, this bit determines whether the -STSCHG input pin is used to activate the IRQ15 pin in conjunction with the IRQ15 Is RI Out bit (**Misc Control 2** bit 7, see page 62). This bit is not valid in Memory Card Interface mode.

7.5 Card Status Change

Register Name: **Card Status Change** *Index:* **04h**						*Register Per:* socket *Register Compatibility Type:* 365	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
0	*0*	*0*	*0*	Card Detect Change	Ready Change	Battery Warning Change	Battery Dead Or Status Change
R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0

This register indicates the source of a management interrupt generated by the CL-PD6729.

NOTE: The corresponding bit in the **Management Interrupt Configuration** register must be set to a '1' to enable each specific status change detection.

Bit 0: Battery Dead Or Status Change

0	A transition (from high to low in Memory Card Interface mode or either high to low or low to high in I/O Card Interface mode) on the BVD1/-STSCHG/-RI pin has not occurred since this register was last read.
1	A transition on the BVD1/-STSCHG/-RI pin has occurred.

In Memory Card Interface mode, this bit is set to a '1' when the BVD1/-STSCHG/-RI pin (see page 13) changes from high to low, indicating a battery dead condition. In I/O Card Interface mode, this bit is set to a '1' when the BVD1/-STSCHG/-RI pin changes from either high to low or low to high. In I/O Card Interface mode, the function of this bit is not affected by bit 7 of the **Interrupt and General Control** register. This bit is reset to a '0' whenever this register is read.

Bit 1: Battery Warning Change

0	A transition (from high to low) on the BVD2/-SPKR/-LED pin has not occurred since this register was last read.
1	A transition on the BVD2/-SPKR/-LED pin has occurred.

In Memory Card Interface mode, this bit is set to a '1' when the BVD2/-SPKR/-LED pin changes from high to low, indicating a battery warning. This bit is not valid in I/O Card Interface mode. This bit is reset to a '0' whenever this register is read.

Bit 2: Ready Change

0	A transition on the RDY/-IREQ pin has not occurred since this register was last read.
1	A transition on the RDY/-IREQ pin has occurred.

In Memory Card Interface mode, this bit is a '1' when a change has occurred on the RDY/-IREQ pin (see page 12). In I/O Card Interface mode, this bit always reads a '0'. This bit is reset to a '0' whenever this register is read.

Bit 3: Card Detect Change

0	A transition on neither the -CD1 nor the -CD2 pin has occurred since this register was last read.
1	A transition on either the -CD1 or the -CD2 pin or both has occurred.

This bit is set to a '1' when a change has occurred on the -CD1 or -CD2 pin (see page 12). This bit is reset to a '0' whenever this register is read.

7.6 Management Interrupt Configuration

Register Name: **Management Interrupt Configuration** *Register Per:* socket
Index: **05h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Management IRQ				Card Detect Enable	Ready Enable	Battery Warning Enable	Battery Dead Or Status Change Enable
RW:0000				RW:0	RW:0	RW:0	RW:0

This register controls which status changes cause management interrupts as well as at which pin the management interrupts will appear.

Bit 0: Battery Dead Or Status Change Enable

0	Battery Dead Or Status Change management interrupt disabled.
1	If Battery Dead Or Status Change bit is a '1', a management interrupt will occur.

When this bit is a '1', a management interrupt will occur when the **Card Status Change** register's Battery Dead Or Status Change bit (see page 45) is a '1'. This allows management interrupts to be generated on changes in level of the BVD1/-STSCHG/-RI pin.

Bit 1: Battery Warning Enable

0	Battery Warning Change management interrupt disabled.
1	If Battery Warning Change bit is a '1', a management interrupt will occur.

When this bit is a '1', a management interrupt will occur when the **Card Status Change** register's Battery Warning Change bit (see page 45) is a '1'. This allows management interrupts to be generated on changes in level of the BVD2/-SPKR/-LED pin. This bit is not valid in I/O Card Interface mode.

Bit 2: Ready Enable

0	Ready Change management interrupt disabled.
1	If Ready Change bit is a '1', a management interrupt will occur.

When this bit is a '1', a management interrupt will occur when the **Card Status Change** register's Ready Change bit (see page 45) is a '1'. This allows management interrupts to be generated on changes in level of the RDY/-IREQ pin.

Bit 3: Card Detect Enable

0	Card Detect Change management interrupt disabled.
1	If Card Detect Change bit is a '1', a management interrupt will occur.

When this bit is a '1', a management interrupt will occur when the **Card Status Change** register's Card Detect Change bit (see page 45) is a '1'. This allows management interrupts to be generated on changes in level of the -CD1 and -CD2 pins.

Bits 7-4: Management IRQ

0000	IRQ disabled
0001	Reserved
0010	Reserved
0011	IRQ3 (INTA#)
0100	IRQ4 (INTB#)
0101	IRQ5 (INTC#)
0110	Reserved
0111	IRQ7 (INTD#)
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14 (This output can alternately be used as external clock input.)
1111	IRQ15 (This output can alternately be used as ring indicate output.)

These bits determine which interrupt pin will be used for card status change management interrupts.

7.7 Mapping Enable

Register Name: **Mapping Enable** *Index:* **06h**						*Register Per:* socket *Register Compatibility Type:* 365	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
I/O Map 1 Enable	I/O Map 0 Enable	*Compatibility Bit*	Memory Map 4 Enable	Memory Map 3 Enable	Memory Map 2 Enable	Memory Map 1 Enable	Memory Map 0 Enable
RW:0	RW:0	R:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0: Memory Map 0 Enable

0	Memory Window Mapping registers for Memory Window 0 disabled.
1	Memory Window Mapping registers for Memory Window 0 enabled.

When this bit is a '1', the Memory Window Mapping registers for Memory Window 0 are enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 1: Memory Map 1 Enable

0	Memory Window Mapping registers for Memory Window 1 disabled.
1	Memory Window Mapping registers for Memory Window 1 enabled.

When this bit is a '1', the Memory Window Mapping registers for Memory Window 1 are enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 2: Memory Map 2 Enable

0	Memory Window Mapping registers for Memory Window 2 disabled.
1	Memory Window Mapping registers for Memory Window 2 enabled.

When this bit is a '1', the Memory Window Mapping registers for Memory Window 2 are enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 3: Memory Map 3 Enable

0	Memory Window Mapping registers for Memory Window 3 disabled.
1	Memory Window Mapping registers for Memory Window 3 enabled.

When this bit is a '1', the Memory Window Mapping registers for Memory Window 3 are enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 4: Memory Map 4 Enable

0	Memory Window Mapping registers for Memory Window 4 disabled.
1	Memory Window Mapping registers for Memory Window 4 enabled.

When this bit is a '1', the Memory Window Mapping registers for Memory Window 4 are enabled and the controller will respond to memory accesses in the memory space defined by those registers.

Bit 6: I/O Map 0 Enable

0	I/O Window Mapping registers for I/O Window 0 disabled.
1	I/O Window Mapping registers for I/O Window 0 enabled.

When this bit is a '1', the I/O Window Mapping registers for I/O Window 0 are enabled and the controller will respond to I/O accesses in the I/O space defined by those registers.

Bit 7: I/O Map 1 Enable

0	I/O Window Mapping registers for I/O Window 1 disabled.
1	I/O Window Mapping registers for I/O Window 1 enabled.

When this bit is a '1', the I/O Window Mapping registers for I/O Window 1 are enabled and the controller will respond to I/O accesses in the I/O space defined by those registers.

8. I/O WINDOW MAPPING REGISTERS

CAUTION: Be sure that the I/O windows do not map to the **Base Address 0** register programmed at offset 10h.

8.1 I/O Window Control

Register Name: **I/O Window Control** *Register Per:* socket
Index: **07h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Timing Register Select 1	*Compatibility Bit*	Auto-Size I/O Window 1	I/O Window 1 Size	Timing Register Select 0	*Compatibility Bit*	Auto-Size I/O Window 0	I/O Window 0 Size
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0: I/O Window 0 Size

0	8-bit data path to I/O Window 0.
1	16-bit data path to I/O Window 0.

When bit 1 if this register is a '0', this bit determines the width of the data path for I/O Window 0 accesses to the card. When bit 1 is a '1', this bit is ignored.

Bit 1: Auto-Size I/O Window 0

0	I/O Window 0 Size (see bit 0 of this register) determines the data path for I/O Window 0 accesses.
1	The data path to I/O Window 0 is determined by the -IOIS16 level returned by the card.

This bit controls the method that the width of the data path for I/O Window 0 accesses to the card is determined. Note that when this bit is a '1', the -IOIS16 signal (see page 12) determines the width of the data path to the card.

Bit 3: Timing Register Select 0

0	Accesses made with timing specified in Timer Set 0 registers.
1	Accesses made with timing specified in Timer Set 1 registers.

This bit determines the access timing specification (see Chapter 11) for I/O Window 0.

Bit 4: I/O Window 1 Size

0	8-bit data path to I/O Window 1.
1	16-bit data path to I/O Window 1.

When bit 5 of this register is a '0', this bit determines the width of the data path for I/O Window 1 accesses to the card. When bit 5 is a '1', this bit is ignored.

Bit 5: Auto-Size I/O Window 1

0	I/O Window 1 Size (see bit 4 of this register) determines the data path for I/O Window 1 accesses.
1	The data path to I/O Window 1 will be determined based on -IOIS16 returned by the card.

This bit controls the method that the width of the data path for I/O Window 1 accesses to the card is determined. Note that when this bit is a '1', the -IOIS16 signal (see page 12) determines the width of the data path to the card. This bit must be set to a '1' for correct ATA mode operation (see Chapter 12).

Bit 7: Timing Register Select 1

0	Accesses made with timing specified in Timer Set 0.
1	Accesses made with timing specified in Timer Set 1.

This bit determines the access timing specification (see Chapter 11) for I/O Window 1.

8.2 System I/O Map 0-1 Start Address Low

Register Name: **System I/O Map 0-1 Start Address Low** *Register Per:* socket
Index: **08h, 0Ch** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Start Address 7-0							
RW:00000000							

There are two separate System I/O Map Start Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System I/O Map Start Address Low
08h	System I/O Map 0 Start Address Low
0Ch	System I/O Map 1 Start Address Low

Bits 7-0: Start Address 7-0

This register contains the least-significant byte of the address that specifies where in the I/O space the corresponding I/O map will begin. I/O accesses that are equal or above this address and equal or below the corresponding System I/O Map End Address will be mapped into the I/O space of the corresponding PCMCIA card.

The most-significant byte is located in the **System I/O Map 0-1 Start Address High** register.

8.3 System I/O Map 0-1 Start Address High

Register Name: **System I/O Map 0-1 Start Address High** *Register Per:* socket
Index: **09h, 0Dh** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Start Address 15-8							
RW:00000000							

There are two separate System I/O Map Start Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System I/O Map Start Address High
09h	System I/O Map 0 Start Address High
0Dh	System I/O Map 1 Start Address High

Bits 15-8: Start Address 15-8

This register contains the most-significant byte of the Start Address. See the description of the Start Address field associated with bits 7-0 of the **System I/O Map 0-1 Start Address Low** register.

8.4 System I/O Map 0-1 End Address Low

Register Name: **System I/O Map 0-1 End Address Low** *Register Per:* socket
Index: **0Ah, 0Eh** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
End Address 7-0							
RW:00000000							

There are two separate System I/O Map End Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System I/O Map End Address Low
0Ah	System I/O Map 0 End Address Low
0Eh	System I/O Map 1 End Address Low

Bits 7-0: End Address 7-0

This register contains the least-significant byte of the address that specifies where in the I/O space the corresponding I/O map will end. I/O accesses that are equal or below this address and equal or above the corresponding System I/O Map Start Address will be mapped into the I/O space of the corresponding PCMCIA card.

The most-significant byte is located in the **System I/O Map 0-1 End Address High** register.

8.5 System I/O Map 0-1 End Address High

Register Name: **System I/O Map 0-1 End Address High** *Register Per:* socket
Index: **0Bh, 0Fh** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
End Address 15-8							
RW:00000000							

There are two separate System I/O Map End Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System I/O Map End Address High
0Bh	System I/O Map 0 End Address High
0Fh	System I/O Map 1 End Address High

Bits 15-8: End Address 15-8

This register contains the most-significant byte of the End Address. See the description of the End Address field associated with bits 7-0 of the **System I/O Map 0-1 End Address Low** register.

8.6 Card I/O Map 0-1 Offset Address Low

Register Name: **Card I/O Map 0-1 Offset Address Low** *Register Per:* socket
Index: **36h, 38h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Offset Address 7-1							*0*[a]
RW:0000000							RW:0

[a] This bit must be programmed to '0'.

There are two separate Card I/O Map Offset Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Card I/O Map Offset Address Low
36h	Card I/O Map 0 Offset Address Low
38h	Card I/O Map 1 Offset Address Low

Bits 7-1: Offset Address 7-1

This register contains the least-significant byte of the quantity that will be added to the system I/O address that determines where in the PCMCIA card's I/O map the I/O access will occur.

The most-significant byte is located in the **Card I/O Map 0-1 Offset Address High** register.

8.7 Card I/O Map 0-1 Offset Address High

Register Name: **Card I/O Map 0-1 Offset Address High** *Register Per:* socket
Index: **37h, 39h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Offset Address 15-8							
RW:00000000							

There are two separate Card I/O Map Offset Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Card I/O Map Offset Address High
37h	Card I/O Map 0 Offset Address High
39h	Card I/O Map 1 Offset Address High

Bits 15-8: Offset Address 15-8

This register contains the most-significant byte of the Offset Address. See the description of the End Address field associated with bits 7-1 of the **Card I/O Map 0-1 Offset Address Low** register.

9. MEMORY WINDOW MAPPING REGISTERS

The following information about the memory map windows is important:

- The memory window mapping registers determine where in the PCI memory space and PC card memory space accesses will occur. There are five memory windows that can be used independently.
- The memory windows are enabled and disabled using the **Mapping Enable** register (see page 48).
- To specify where in the PCI space a memory window is mapped, start and end addresses are specified. A memory window is selected whenever the appropriate Memory Map Enable bit (see page 48) is set and the following conditions are true:
  - The PCI address is greater than or equal to the appropriate **System Memory Map Start Address** register (see page 54).
  - The PCI address is less than or equal to the appropriate **System Memory Map End Address** register (see page 55).
  - The **System Memory Map Upper Address** register (see page 67) is equal to the upper PCI address.
- Start and end addresses are specified with PCI Address bits 31-12. This sets the minimum size of a memory window to 4K bytes. Memory windows are specified in the PCI memory address space.
- To ensure proper operation, none of the memory windows can overlap in the PCI address space.

9.1 System Memory Map 0-4 Start Address Low

Register Name: **System Memory Map 0-4 Start Address Low** *Register Per:* socket
Index: **10h, 18h, 20h, 28h, 30h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Start Address 19-12							
RW:00000000							

There are five separate System Memory Map Start Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System Memory Map Start Address Low
10h	System Memory Map 0 Start Address Low
18h	System Memory Map 1 Start Address Low
20h	System Memory Map 2 Start Address Low
28h	System Memory Map 3 Start Address Low
30h	System Memory Map 4 Start Address Low

Bits 7-0: Start Address 19-12

This register contains the least-significant byte of the address that specifies where in the memory space the corresponding memory map will begin. Memory accesses that are equal or above this address and equal or below the corresponding System Memory Map End Address will be mapped into the memory space of the corresponding PCMCIA card.

The most-significant four bits are located in the **System Memory Map 0-4 Start Address High** register.

9.2 System Memory Map 0-4 Start Address High

Register Name: **System Memory Map 0-4 Start Address High** *Register Per:* socket
Index: **11h, 19h, 21h, 29h, 31h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Window Data Size	*Compatibility Bit*	*Scratchpad Bits*		Start Address 23-20			
RW:0	RW:0	RW:00		RW:0000			

There are five separate System Memory Map Start Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System Memory Map Start Address High
11h	System Memory Map 0 Start Address High
19h	System Memory Map 1 Start Address High
21h	System Memory Map 2 Start Address High
29h	System Memory Map 3 Start Address High
31h	System Memory Map 4 Start Address High

Bits 3-0: Start Address 23-20

This field contains the most-significant four bits of the Start Address. See the description of the Start Address field associated with bits 7-0 of the **System Memory Map 0-4 Start Address Low** register.

Bit 7: Window Data Size

0	8-bit data path to the card.
1	16-bit data path to the card.

This bit determines the data path size to the card.

9.3 System Memory Map 0-4 End Address Low

Register Name: **System Memory Map 0-4 End Address Low** *Register Per:* socket
Index: **12h, 1Ah, 22h, 2Ah, 32h** *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
End Address 19-12							
RW:00000000							

There are five separate System Memory Map End Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System Memory Map End Address Low
12h	System Memory Map 0 End Address Low
1Ah	System Memory Map 1 End Address Low
22h	System Memory Map 2 End Address Low
2Ah	System Memory Map 3 End Address Low
32h	System Memory Map 4 End Address Low

Bits 7-0: End Address 19-12

This register contains the least-significant byte of the address that specifies where in the memory space the corresponding memory map will end. Memory accesses that are equal or below this address and equal or above the corresponding System Memory Map Start Address will be mapped into the memory space of the corresponding PCMCIA card.

The most-significant four bits are located in the **System Memory Map 0-4 End Address High** register.

9.4 System Memory Map 0-4 End Address High

Register Name: **System Memory Map 0-4 End Address High** — *Register Per:* socket
Index: **13h, 1Bh, 23h, 2Bh, 33h** — *Register Compatibility Type:* 365

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Card Timer Select		*Scratchpad Bits*		End Address 23-20			
RW:00		RW:00		RW:0000			

There are five separate System Memory Map End Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	System Memory Map End Address High
13h	System Memory Map 0 End Address High
1Bh	System Memory Map 1 End Address High
23h	System Memory Map 2 End Address High
2Bh	System Memory Map 3 End Address High
33h	System Memory Map 4 End Address High

Bits 3-0: End Address 23-20

This field contains the most-significant four bits of the End Address. See the description of the End Address field associated with bits 7-0 of the **System Memory Map 0-4 End Address Low** register. Note that the upper memory addresses are stored in the **System Memory Map Upper Address** register.

Bits 7-6: Card Timer Select

00	Selects Timer Set 0.
01	Selects Timer Set 1.
10	Selects Timer Set 1.
11	Selects Timer Set 1.

This field selects the timer set. Timer Set 0 and 1 reset to values compatible with standard PCI and three-wait-state cycles (see page 74).

9.5 Card Memory Map 0-4 Offset Address Low

Register Name: **Card Memory Map 0-4 Offset Address Low** *Register Per:* socket
Index: **14h, 1Ch, 24h, 2Ch, 34h** *Register Compatibility Type:* 365

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Offset Address 19-12							
RW:00000000							

There are five separate Card Memory Map Offset Address Low registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Card Memory Map Offset address Low
14h	Card Memory Map 0 Offset Address Low
1Ch	Card Memory Map 1 Offset Address Low
24h	Card Memory Map 2 Offset Address Low
2Ch	Card Memory Map 3 Offset Address Low
34h	Card Memory Map 4 Offset Address Low

Bits 7-0: Offset Address 19-12

This register contains the least-significant byte of the quantity that will be added to the system memory address that determines where in the PCMCIA card's memory map the memory access will occur.

The most-significant six bits are located in the **Card Memory Map 0-4 Offset Address High** register.

9.6 Card Memory Map 0-4 Offset Address High

Register Name: **Card Memory Map 0-4 Offset Address High** *Register Per:* socket
Index: **15h, 1Dh, 25h, 2Dh, 35h** *Register Compatibility Type:* 365

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write Protect	REG Setting	Offset Address 25-20					
RW:0	RW:0	RW:000000					

There are five separate Card Memory Map Offset Address High registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Memory Map Address Offset High
15h	Card Memory Map 0 Offset Address High
1Dh	Card Memory Map 1 Offset Address High
25h	Card Memory Map 2 Offset Address High
2Dh	Card Memory Map 3 Offset Address High
35h	Card Memory Map 4 Offset Address High

Bits 5-0: Offset Address 25-20

This field contains the most-significant six bits of the Offset Address. See the description of the Offset Address field associated with bits 7-0 of the **Card Memory Map 0-4 Offset Address Low** register.

Bit 6: REG Setting

0	-REG (see page 11) is not active for accesses made through this window.
1	-REG is active for accesses made through this window.

This bit determines whether -REG (see page 11) is active for accesses made through this window. Card Information Structure (CIS) memory is accessed by setting this bit to a ‘1’.

Bit 7: Write Protect

0	Writes to the card through this window are allowed.
1	Writes to the card through this window are inhibited.

This bit determines whether writes to the card through this window are allowed.

10. EXTENSION REGISTERS

10.1 Misc Control 1

Register Name: **Misc Control 1** *Register Per:* socket
Index: **16h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Inpack Enable	*Scratchpad Bits*		Speaker Enable	Pulse System IRQ	Pulse Management Interrupt	V_{CC} 3.3V	Multimedia Enable
RW:0	RW:00		RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0: Multimedia Enable

0	Socket address lines are normal.
1	Socket address lines A[25:4] are high-impedance.

This bit tristates socket address lines A[25:4]. All other aspects of the socket are not affected by this bit.

NOTE: Bit 7 in the Extended register 25h, the **Misc Control 3** register must be set to a '1' for this bit to enable tristating of address lines [25:4].

Bit 1: V_{CC} 3.3V

0	-VCC_5 activated when card power is to be applied.
1	-VCC_3 activated when card power is to be applied.

This bit determines which output pin is used to enable V_{CC} power to the socket when card power is applied; this bit is used in conjunction with bits 5-4 of the **Power Control** register (see page 41).

Bit 2: Pulse Management Interrupt

0	Interrupts are passed to the IRQ[XX] pin as level-sensitive.
1	When an interrupt occurs, the IRQ[XX] pin is driven with the pulse train shown in Figure 10-1 and allows for interrupt sharing.

This bit selects Level or Pulse mode operation of the IRQ[XX] pin (see page 9). Note that a clock must be present on PCI_CLK or IRQ14/EXT_CLK for pulsed interrupts to work. Refer to Section 13.3.2 for more information on interrupt timing.

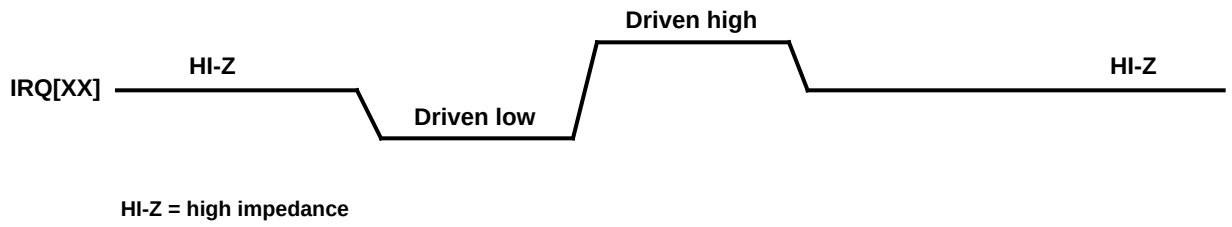


Figure 10-1. Pulse Mode Interrupts

Bit 3: Pulse System IRQ

0	Interrupts are passed to the IRQ[XX] pin as level-sensitive.
1	When an interrupt occurs, the IRQ[XX] pin is driven with the pulse train shown in Figure 10-1 and allows for interrupt sharing.

This bit selects Level or Pulse mode operation of the IRQ[XX] pins (see page 9).

Bit 4: Speaker Enable

0	SPKR_OUT* is three-stated.
1	SPKR_OUT* is driven from the XOR of -SPKR from each enabled socket.

This bit determines whether the card -SPKR pin will drive SPKR_OUT* (see page 14).

Bit 7: Inpack Enable

0	No effect.
1	No effect.

The -INPACK function is not applicable in PCI bus environments. This bit is provided for compatibility with other Cirrus Logic products. Its setting has no effect on operations of the CL-PD6729.

10.2 FIFO Control

Register Name: **FIFO Control** *Index:* **17h**							*Register Per:* socket *Register Compatibility Type:* ext.
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
FIFO Status / Flush FIFO	*Scratchpad Bits*						
RW:1	RW:0000000						

Bit 7: FIFO Status / Flush FIFO

Value	I/O Read	I/O Write
0	FIFO not empty	No operation occurs (default at reset)
1	FIFO empty	Flush the FIFO

This bit controls FIFO operation and reports FIFO status. When this bit is set to a ‘1’ during write operations, all data in the FIFO is lost. During read operations, when this bit is a ‘1’, the FIFO is empty. During read operations when this bit is a ‘0’, the FIFO has valid data.

This bit is used to ensure the FIFO is empty before changing any registers; registers should not be modified while the write FIFO is not empty.

FIFO contents will be lost whenever any of the following occur:

- RST# pin (see page 9) is a ‘0’.
- The card is removed.
- V_{CC} Power bit (see page 42) is programmed to a ‘0’.

10.3 Misc Control 2

Register Name: **Misc Control 2** *Index:* **1Eh**						*Register Per:* chip *Register Compatibility Type:* ext.	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
IRQ15/ RI_OUT* Is RI Out	*Reserved*		Reserved	5V Core	Suspend Mode	Low-Power Dynamic Mode	External Clock Enable
RW:0	RW:00		RW:0	RW:0	RW:0	RW:1	RW:0

Bit 0: External Clock Enable

0	External clock is disabled; clocking of socket interfaces provided by PCI_CLK.
1	IRQ14/EXT_CLK pin will be used as an external clock input to provide clocking of socket interfaces.

This bit determines whether the external clock option is enabled. When set to a '1', a clock supplied to IRQ14/EXT_CLK will be internally divided by two and used as the internal clock for the socket interfaces. This feature facilitates PCMCIA transfer cycles when the PCI bus clock is stopped to conserve power. When set to a '0', the PCI_CLK input is divided by two and used as the internal clock, which drives the socket interfaces and specifies their timing.

Bit 1: Low-Power Dynamic Mode

0	Clock runs always.
1	Normal operation, stop clock when possible.

This bit determines whether Low-power Dynamic mode is enabled. Leaving this bit set to '1' allows automatic reduction in power consumption during periods of inactivity.

Bit 2: Suspend Mode

0	Normal operation.
1	Stop internal clock, enable all Low-power modes, and disable socket access.

This bit enables Suspend mode. No registers other than this (index 1E) should be written when in Suspend mode. Ability to read registers in Suspend mode should not be expected. Access cycles to cards in sockets are not allowed in Suspend mode.

Bit 3: 5V Core

0	Normal operation: use when CORE_VDD pin is connected to 3.3 volts.
1	Selects input thresholds for use when 5.0 volts is connected to the CL-PD6729 CORE_VDD pin.

This bit selects input threshold circuits. This bit must be set to a '1' when the CORE_VDD pin is connected to 5.0 volts to provide TTL-compatible input thresholds at card socket.

Bit 7: IRQ15/RI_OUT* Is RI Out

0	Normal IRQ15 operation on the IRQ15/RI_OUT* pin.
1	IRQ15/RI_OUT* is connected to ring indicate pin on the system logic.

This bit determines the function of the IRQ15/RI_OUT* pin. When this bit is set to a '1', IRQ15/RI_OUT* can be used to trigger restoration of system activity when a high-to-low change is detected on the BVD1/-STSCHG/-RI pin.

10.4 Chip Information

Register Name: **Chip Information** *Register Per:* chip
Index: **1Fh** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Cirrus Logic Host-Adapter Identification		CL-PD6729 Revision Level					
R:11		R:nnnnnnnn[a]					

[a] This read-only value depends on the revision level of the CL-PD6729 chip. A value of 21h/E1h indicates the chip uses extended registers 34h-3Bh to indicate chip revision and features.

Bits 5-0: CL-PD6729 Revision Level

This field identifies the revision of the controller. Contact Cirrus Logic for more information on revision levels for the CL-PD6729.

Bits 7-6: Cirrus Logic Host-Adapter Identification

00	Second read after I/O write to this register.
11	First read after I/O write to this register.

This field identifies a Cirrus Logic host-adapter device. After chip reset or doing an I/O write to this register, the first read of this register will return a 11b. On the next read, this field will be 00b. This pattern of toggling data on subsequent reads can be used by software to determine presence of a Cirrus Logic host adapter in a system or to determine occurrence of a device reset.

10.5 ATA Control

Register Name: **ATA Control** *Index:* **26h**						*Register Per:* socket *Register Compatibility Type:* ext.	
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
A25/CSEL	A24/M/S*	A23/VU	A22	A21	*Scratchpad Bit*	Speaker Is LED Input	ATA Mode
RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0: ATA Mode

0	Normal operation.
1	Configures the socket interface to handle ATA-type disk drives.

This bit reconfigures the particular socket as an ATA drive interface. Refer to Table 12-1 on page 77 for PCMCIA socket pin definitions in ATA mode.

Bit 1: Speaker Is LED Input

0	Normal operation.
1	The PCMCIA -SPKR pin will be used to drive LED_OUT* if Drive LED Activity Enable (see page 66) is set.

This bit changes the function of the BVD2/-SPKR/-LED pin (see page 13) from digital speaker input to disk status LED input. When in I/O Card Interface mode or ATA mode, setting this bit to a '1' reconfigures the BVD2/-SPKR/-LED input pin to serve as a -LED input from the socket.

NOTE: This bit should be set to a '0' if in Memory Card Interface mode.

Bit 3: A21

In ATA mode, the value in this bit is applied to the ATA A21 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PCMCIA 2.1 standard can be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 4: A22

In ATA mode, the value in this bit is applied to the ATA A22 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PCMCIA 2.1 standard can be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 5: A23/VU

In ATA mode, the value in this bit is applied to the ATA A23 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PCMCIA 2.1 standard can be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 6: A24/M/S*

In ATA mode, the value in this bit is applied to the ATA A24 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PCMCIA 2.1 standard can be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

Bit 7: A25/CSEL

In ATA mode, the value in this bit is applied to the ATA A25 pin and is vendor-specific. Certain ATA drive vendor-specific performance enhancements beyond the PCMCIA 2.1 standard can be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.

10.6 Extended Index

Register Name: **Extended Index** *Register Per:* socket
Index: **2Eh** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Extended Index							
RW:00000000							

This register controls which of the following registers at index 2Fh can be accessed:

Register Name at Index 2Fh	Extended Index
Scratchpad	00h
Reserved	01h
Reserved	02h
Extension Control 1	03h
Reserved	04h
System Memory Map 0 Upper Address	05h
System Memory Map 1 Upper Address	06h
System Memory Map 2 Upper Address	07h
System Memory Map 3 Upper Address	08h
System Memory Map 4 Upper Address	09h
Reserved	0Ah
Misc. Control 3	25h
Mask Revision Byte	34h
Product ID Byte	35h
Device Capability Byte A	36h
Device Capability Byte B	37h
Device Implementation Byte A	38h
Device Implementation Byte B	39h
Device Implementation Byte C	3Ah
Device Implementation Byte D	3Bh

For information on how to access these registers, see Section 3.2.

10.7 Extended Data

Register Name: **Extended Data**							*Register Per:* socket
Index: **2Fh**							*Register Compatibility Type:* ext.
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Extended Data							

The data in this register allows the registers indicated by the **Extended Index** register to be read and written. The value of this register is the value of the register selected by the **Extended Index** register.

10.7.1 Extension Control 1

Register Name: **Extension Control 1**							*Register Per:* socket
Index: **2Fh**			*Extended Index:* **03h**				*Register Compatibility Type:* ext.
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved		Pull-Up Control	Invert Management IRQ Output	Invert Card IRQ Output	LED Activity Enable	Auto Power Clear	V_{CC} Power Lock
RW:00		RW:0	RW:0	RW:0	RW:0	RW:0	RW:0

Bit 0: V_{CC} Power Lock

0	The V_{CC} Power bit (bit 4 of **Power Control** register) is not locked.
1	The V_{CC} Power bit (bit 4 of **Power Control** register) cannot be changed by software.

This bit can be used to prevent card drivers from overriding the Socket Services' task of controlling power to the card, thus preventing situations where cards are powered incorrectly.

Bit 1: Auto Power Clear

0	The V_{CC} Power bit (bit 4 of **Power Control** register) is reset to '0' when the card is removed.
1	The V_{CC} Power bit (bit 4 of **Power Control** register) is not affected by card removal.

Bit 2: LED Activity Enable

0	LED activity disabled.
1	LED activity enabled.

This bit allows the LED_OUT* pin to reflect any activity in the card. Whenever PCMCIA cycles are in process to or from a card in either socket, LED_OUT* will be active low.

Bit 3: Invert Card IRQ Output

0	The card IRQ is active-high.
1	The card IRQ is active-low and open-drain.

This bit changes the active-high, ISA-type card IRQ level to an active-low, open-collector output that complies with PCI bus requirements.

Bit 4: Invert Management IRQ Output

0	The management IRQ is active-high.
1	The management IRQ is active-low and open-drain.

This bit changes the active-high, ISA-type management IRQ level to an active-low, open-collector output that complies with PCI bus requirements.

Bit 5: Pull-Up Control

0	Pull-ups on VS2, VS1, CD2, and CD1 are in use.
1	Pull-ups on VS2, VS1, CD2, and CD1 are turned off.

This bit turns off the pull-ups on VS2, VS1, CD2, and CD1. Turning off these pull-ups can be used in addition to Suspend mode to even further reduce power when cards are inserted but no card accessibility is required. Even though power may or may not still be applied, all pull-ups and their associated inputs will be disabled.

NOTE: Insertion or removal of a card cannot be determined when this bit is set to a '1'. Also, when a card is already in the socket, a card detect interrupt will be generated when this bit is changed from a '0' to '1'.

10.7.2 System Memory Map 0-4 Upper Address

Register Name: **System Memory Map 0-4 Upper Address** — *Register Per:* socket
Index: **2Fh** — *Extended Index:* **05h–09h** — *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Upper Address							
RW:00000000							

These bits are used in comparing PCI Address bits 31-24 for each memory window (0-4). These bits are used in conjunction with the **System Memory Map 0-4 Start Address** and **System Memory Map 0-4 End Address** registers.

10.7.3 Misc Control 3

Register Name: **Misc Control 3** — *Register Per:* socket
I/O Index: **2Fh** *Extended Index:* **25h** — *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Multimedia Arm	Multimedia Expand	*Reserved*					
R/W:0	R/W:0						

Bit 6 — Multimedia Expand

0	Multimedia expand disabled.
1	Multimedia expand enabled.

This bit allows 24-bit video from the PC Card. If the Multimedia Arm bit and Multimedia Enable bit are both set to '1', this bit causes CE2 and D[15:8] to be tristated on the 16-bit PC Card bus, and also tristates A[25:4].

Bit 7 — Multimedia Arm

0	Multimedia Arm disabled.
1	Multimedia Arm enabled.

No multimedia operation can take place without first setting this bit to ‘1’; the bit provides an overriding control mechanism. By setting only bit 0 of index 16h, the Multimedia Arm bit ensures that multimedia operation is not inadvertently set by software or point enablers.

10.8 Device Identification and Implementation Scheme

There are four byte-wide registers with read-only device information, and four byte-wide read/write registers that contain specific system-implementation information. These registers are found in revisions of the CL-PD6729 that have the value 21h/E1h in the Chip Information register (index 1F).

10.8.1 Mask Revision Byte

Register Name: **Mask Revision Byte** *Register Per:* chip
Index: **2Fh** *Extended Index:* **34h** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Mask Revision							
R:nnnnnnnn[a]							

[a] Contact Cirrus Logic representatives for the value corresponding to a particular revision of the CL-PD6729.

Bits 7:0 — Mask Revision

These bits indicate the mask revision of the device. Contact Cirrus Logic representatives for information on correlating revision numbers with the value of this field.

10.8.2 Product ID Byte

Register Name: **Product ID Byte** *Index:* **2Fh**			*Extended Index:* **35h**			*Register Per:* chip *Register Compatibility Type:* ext.	
Bit 15	*Bit 14*	*Bit 13*	*Bit 12*	*Bit 11*	*Bit 10*	*Bit 9*	*Bit 8*
Family Code				Product Code			
R:0	R:0	R:1	R:0	R:0	R:0	R:0	R:0

Bits 15:12 — Family Code

A value of '2h' indicates the CL-PD6729 family.

Bits 11:8 — Product Code

These bits indicate the product code of the device within its family.

Product Codes — CL-PD6729 Family (Family Code 2h)

0h	CL-PD6729 PCI/PCMCIA Controller, dual isolated sockets, 208 pin
1h-Fh	Reserved for future use for CL-PD6729 devices

10.8.3 Device Capability Byte A

Register Name: **Device Capability Byte A** *Index:* **2Fh**			*Extended Index:* **36h**			*Register Per:* chip *Register Compatibility Type:* ext.	
Bit 23	*Bit 22*	*Bit 21*	*Bit 20*	*Bit 19*	*Bit 18*	*Bit 17*	*Bit 16*
Per Skt LED	RFU	GPSTB Capable	RFU	Slave DMA	IDE Interface	# Sockets 1	# Sockets 0
R:0	R:0	R:1	R:0	R:0	R:0	R:0	R:1

Bit 23: Per-Socket LED

A '0' indicates that the CL-PD6729 uses a single LED output to indicate status on both sockets.

Bit 22: RFU (Reserved for Future Use)

Reserved for future use.

Bit 21: GPSTB Capable

A value of '1' in this field is intended to indicate that a Cirrus Logic device supports general-purpose strobe. Note that even though the CL-PD6729 may report this bit as '1', it DOES NOT support the general-purpose strobe.

Bit 20: RFU (Reserved for Future Use)

Reserved for future use.

Bit 19: Slave DMA

A '0' at this bit indicates that the CL-PD6729 does not act as an DMA slave.

Bit 18: IDE Interface

A value of '0' indicates that this device does not provide a separate IDE interface. Note that PCMCIA-ATA drives are supported through the PC Card interfaces on the CL-PD6729.

Bit 17:16: Number of Sockets Supportable By Device

This bit field is '0', indicating the CL-PD6729 supports two PC Card sockets.

10.8.4 Device Capability Byte B

Register Name: **Device Capability Byte B** *Register Per:* chip
Index: **2Fh** *Extended Index:* **37h** *Register Compatibility Type:* ext.

Bit 31	*Bit 30*	*Bit 29*	*Bit 28*	*Bit 27*	*Bit 26*	*Bit 25*	*Bit 24*
Extended Def's	RFU (ZV)	RFU (ZV)	RFU (ZV)	RFU (CB)	CLKRUN Support	LOCK# Support	CardBus Capable
R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0

Bit 31: Extended Definitions

A value of '0' indicates that there is no extended definition. Description of device capabilities and implementations stops at extended register 3Bh.

Bits 30:27: RFU (Reserved for Future Use)

Reserved for future use.

Bit 26: CLKRUN Support

A '0' indicates that the CL-PD6729 does not output a CLKRUN signal for the PCI Mobile Specification signaling for control of system clock turn on/turn off.

Bit 25: LOCK# Support

A '0' indicates that the CL-PD6729 does not support operations involving the LOCK# signal.

Bit 24: Cardbus Capable

A '0' in this bit indicates that the CL-PD6729 does not support Cardbus transfer cycles on PC Cards.

10.8.5 Device Implementation Byte A

Register Name: **Device Implementation Byte A** *Register Per:* chip
Index: **2Fh** *Extended Index:* **38h** *Register Compatibility Type:* ext.

Bit 39	*Bit 38*	*Bit 37*	*Bit 36*	*Bit 35*	*Bit 34*	*Bit 33*	*Bit 32*
RI_OUT Wired	H/W Sus.Wired	GPSTB B Wired	GPSTB A Wired	VS1/VS2 Wired	Slv. DMA Wired	Sockets Present 1	Sockets Present 0
R/W:0	R/W:0	R/W:0	R/W:0	R/W:1	R/W:0	R/W:0	R/W:1

All bits of this byte are read/write.

Device reset defaults are specific to each device. It is intended that a BIOS write to this byte before launching socket services would set these bits to reflect which features are supported in the system implementation.

Bit 39: RI_OUT Wired

A '1' indicates that in the system implementation, a pin on the device designated as 'RI_OUT' has been connected to ring indicate circuitry. Socket services must set register 1E bit 7 to a '1', thereby enabling this alternate pin definition as it has been wired.

A value of '1' implies that in the system implementation, the RI_OUT*/IRQ15 pin is not connected to the ISA bus IRQ15 line, but is instead connected to an SMI-type system function designed to wake up a system on modem ring.

Bit 38: Hardware Suspend Wired

A '1' indicates that in the system implementation, a pin on the device designated as a hardware control of suspend for deep power saving has been connected to system circuitry designed for power management. Since the CL-PD6729 has no hardware suspend pin, this bit should remain cleared to '0'.

10.8.6 Device Implementation Byte B

Register Name: **Device Implementation Byte B** *Index:* **2Fh**			*Extended Index:* **39h**			*Register Per:* chip *Register Compatibility Type:* ext.	
Bit 47	*Bit 46*	*Bit 45*	*Bit 44*	*Bit 43*	*Bit 42*	*Bit 41*	*Bit 40*
RFU	RF Rated Sockets	VPP_ VCC 1A	VPP 12V Avail	X.V Capable	Y.V Capable	5.0V VCC Capable	3.3V VCC Capable
R/W:0	R/W:1	R/W:0	R/W:1	R/W:0	R/W:0	R/W:1	R/W:1

Bit 47: RFU (Reserved for future use)

Reserved for future use.

Bit 46: RF Rated Sockets

A value of '1' indicates that in the system implementation, the sockets in this systems are designed to handle cards that operate at radio frequencies like cellular fax/modem, pagers, etc. A value of '0' indicates that the sockets in this systems are not designed to handle cards that operate at radio frequencies like cellular fax/modem, pagers, etc.

Bit 45: VPP_VCC 1A

A value of '1' indicates that, in this implementation, the socket can deliver 1 A to each socket's VPP and VPP2 pins when the VPP voltage is set to VCC.

Bit 44: VPP 12 V available

A value of '1' indicates that a VPP voltage of 12 V is supported in this system. A value of '0' indicates that a VPP of 12 V is not supported in this system, meaning VPP voltages of 'VCC' and OV are the only programming voltages available.

Bit 43: X.V capable

A value of '1' indicates that X.X V voltage source is available for the powering of PC cards in this system. A value of '0' indicates that X.X V voltage source is not available for the powering of PC cards in this system.

Bit 42: Y.V capable

A value of '1' indicates that Y.Y V voltage source is available for the powering of PC cards in this system. A value of '0' indicates that Y.Y V voltage source is not available for the powering of PC cards in this system.

Bit 41: 5.0V capable

A value of '1' indicates that 5.0 V voltage source is available for the powering of PC cards in this system. A value of '0' indicates that 5.0 V voltage source is not available for the powering of PC-cards in this system, and that the PC card sockets only operate at other available voltages indicated by bits 43:41. Systems that only supported 5 V cards set bit 41 to '1' and clear bits 43, 42, and 40 to '0'.

Bit 40: 3.3V capable

A value of '1' indicates that 3.3 V voltage source is available for the powering of PC cards in this system. A value of '0' indicates that 3.3 V voltage source is not available for the powering of PC cards in this system. System designs that support both 3.3 and 5.0 V cards set bits to '1' and clear bits 43 and 42 to '0'.

10.8.7 Device Implementation Byte C

Register Name: **Device Implementation Byte C** *Index:* **2Fh**			*Extended Index:* **3Ah**			*Register Per:* chip *Register Compatibility Type:* ext.	
Bit 55	*Bit 54*	*Bit 53*	*Bit 52*	*Bit 51*	*Bit 50*	*Bit 49*	*Bit 48*
RFU	RFU (ZV)	RFU (ZV)	ZV Port B Wired	ZV Port A Wired	SPKR Wired	Per Skt LED	LED Wired
R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:1	R/W:0	R/W:0

Bits 55:53 — RFU (Reserved for future use)

Reserved for future use.

Bit 52 — ZV Port B Wired

A value of '1' indicates that in the particular system implementation, Socket B is wired for ZV operation. A value of '0' indicates that Socket B is not wired for ZV operation.

Bit 51 — ZV Port A Wired

A value of '1' indicates that in the particular system implementation, Socket A is wired for ZV operation. A value of '0' indicates that Socket A is not wired for ZV operation.

Bit 50 — SPKR Wired

A value of '1' indicates that in the particular system implementation, a speaker is connected to the SPKR_OUT pin. A value of '0' indicates that a speaker is not connected to the SPKR_OUT pin.

Bit 49 — Per Skt LED

A value of '1' indicates that in the particular system implementation, there are separate status LEDs for each socket being controlled by the device. This bit should remain cleared to '0' as the CL-PD6729 supports a single status LED.

Bit 48 — LED Wired

A value of '1' indicates that in the particular system implementation a status LED has been connected to the LED_OUT# pin. A value of '0' indicates that a status LED is not connected in this system implementation.

10.8.8 Device Implementation Byte D

Register Name: **Device Implementation Byte D** *Register Per:* chip
Index: **2Fh** *Extended Index:* **3Bh** *Register Compatibility Type:* ext.

Bit 63	*Bit 62*	*Bit 61*	*Bit 60*	*Bit 59*	*Bit 58*	*Bit 57*	*Bit 56*
RFU	Clk Opt. Wired	RFU	RFU	RFU	RFU	LOCK# Wired	CLKRUN Wired
R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0

Bit 63 — RFU (Reserved for future use)

Reserved for future use.

Bit 62 — Clk Opt. Wired

A value of '1' indicates that in the particular system implementation, an external clock has been wired to the CL-PD6729 EXT_CLK pin. A value of '0' indicates that an external clock is being connected.

Bits 61:58 — RFU (Reserved for future use)

Reserved for future use.

Bit 57 — LOCK# Wired

A value of '1' indicates that the system the system implementation provides a LOCK# signal to a device. Since the CL-PD6729 does not implement LOCK#, this bit should remain cleared to '0'.

Bit 56 — CLKRUN Wired

A value of '1' indicates that the system implementation wires a CLKRUN signal to a device's CLKRUN pin. supports CLKRUN protocol. Since the CL-PD6729 does not have a CLKRUN pin, this bit should remain cleared to '0'.

10.8.9 External Data (Index 6Fh)

Register Name: **External Data** *Register Per:* chip
Index: **6Fh** *Extended Index:* **0Ah** *Register Compatibility Type:* ext.

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved				Socket B VS2 Input	Socket B VS1 Input	Socket A VS2 Input	Socket A VS1 Input
RW:0000				R:0	R:0	R:0	R:0

Bits 3-0: Socket A/B VS1/VS2 Input

These bits indicate the values of the four voltage sense pins (two for each socket). These values are used to determine the operating voltage capabilities of an inserted card.

11. TIMING REGISTERS

The following information about the timing registers is important:

- All timing registers take effect immediately and should only be changed when the FIFO is empty (see the **FIFO Control** register on page 61).
- Selection of Timer Set 0 or Timer Set 1 register sets is controlled by **I/O Window Control**, bits 3 and 7 (see page 50).

11.1 Setup Timing 0-1

Register Name: **Setup Timing 0-1** *Register Per:* socket
Index: **3Ah, 3Dh** *Register Compatibility Type:* 365

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Setup Prescalar Select		Setup Multiplier Value					
RW:00		RW:000001					

There are two separate Setup Timing registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Setup Timing
3Ah	Setup Timing 0
3Dh	Setup Timing 1

The Setup Timing register for each timer set controls how long a PCMCIA cycle's command (that is, -OE, -WE, -IORD, -IOWR; see page 11) setup time will be, in terms of the number of internal clock cycles.

The overall command setup timing length S is programmed by selecting a 2-bit prescaling value (bits 7-6 of this register) representing weights of 1, 16, 256, or 4096, and then selecting a multiplier value (bits 5-0) to which that prescalar is multiplied to produce the overall command setup timing length according to the following formula:

$$S = (N_{pres} \times N_{val}) + 1$$

The value of S, representing the number of clock cycles for command setup, is then multiplied by the clock period of the internal clock driving the PC card socket interface to determine the actual command setup time (see Section 13.3.3 for further discussion).

Bits 5-0: Setup Multiplier Value

This field indicates an integer value N_{val} from 0 to 63; it is combined with a prescalar value (bits 7-6) to control the length of setup time before a command becomes active.

Bits 7-6: Setup Prescalar Select

00	$N_{pres} = 1$
01	$N_{pres} = 16$
10	$N_{pres} = 256$
11	$N_{pres} = 4096$

This field chooses one of four prescalar values N_{pres} that are combined with the value of the Setup Multiplier Value (bits 5-0) to control the length of setup time before a command becomes active.

11.2 Command Timing 0-1

Register Name: **Command Timing 0-1** *Index:* **3Bh, 3Eh**							*Register Per:* socket *Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Command Prescalar Select		Command Multiplier Value					
RW:00		RW:000101/010100[a]					

[a] Timing set 0 (index 3Bh) resets to 5h, providing a 300-ns nominal PC card command width useable for support of '250-ns' PC cards. Timing set 1 (3Eh) resets to 14h, providing a 900 ns nominal PC card command width.

There are two separate Command Timing registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Command Timing
3Bh	Command Timing 0
3Eh	Command Timing 1

The Command Timing register for each timer set controls how long a PCMCIA cycle's command (that is, -OE, -WE, -IORD, -IOWR; see page 11) active time will be, in terms of the number of internal clock cycles.

The overall command timing length C is programmed by selecting a 2-bit prescaling value (bits 7-6 of this register) representing weights of 1, 16, 256, or 4096, and then selecting a multiplier value (bits 5-0) to which that prescalar is multiplied to produce the overall command timing length according to the following formula:

$$C = (N_{pres} \times N_{val}) + 1$$

The value of C, representing the number of clock cycles for a command, is then multiplied by the clock period of the internal clock driving the PC card interface to determine the actual command active time (see Section 13.3.3 for further discussion).

Bits 5-0: Command Multiplier Value

This field indicates an integer value N_{val} from 0 to 63; it is combined with a prescalar value (bits 7-6) to control the length that a command is active.

Bits 7-6: Command Prescalar Select

00	$N_{pres} = 1$
01	$N_{pres} = 16$
10	$N_{pres} = 256$
11	$N_{pres} = 4096$

This field chooses one of four prescalar values N_{pres} that are combined with the value of the Command Multiplier Value (bits 5-0) to control the length that a command is active.

11.3 Recovery Timing 0-1

Register Name: **Recovery Timing 0-1**							*Register Per:* socket
Index: **3Ch, 3Fh**							*Register Compatibility Type:* 365
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Recovery Prescalar Select		Recovery Multiplier Value					
RW:00		RW:000000					

There are two separate Recover Timing registers, each with identical fields. These registers are located at the following indexes:

Index (Socket A)	Recovery Timing
3Ch	Recovery Timing 0
3Fh	Recovery Timing 1

The Recovery Timing register for each timer set controls how long a PCMCIA cycle's command (that is, -OE, -WE, -IORD, -IOWR; see page 11) recovery time will be, in terms of the number of internal clock cycles.

The overall command recovery timing length R is programmed by selecting a 2-bit prescaling value (bits 7-6 of this register) representing weights of 1, 16, 256, or 4096, and then selecting a multiplier value (bits 5-0) to which that prescalar is multiplied to produce the overall command recovery timing length according to the following formula:

$$R = (N_{pres} \times N_{val}) + 1$$

The value of R, representing the number of clock cycles for command recovery, is then multiplied by the clock period of the internal clock driving the PC card interface to determine the actual command recovery time (see Section 13.3.3 for further discussion).

Bits 5-0: Recovery Multiplier Value

This field indicates an integer value N_{val} from 0 to 63; it is combined with a prescalar value (bits 7-6) to control the length of recovery time after a command is active.

Bits 7-6: Recovery Prescalar Select

00	$N_{pres} = 1$
01	$N_{pres} = 16$
10	$N_{pres} = 256$
11	$N_{pres} = 4096$

This field chooses one of four prescalar values N_{pres} that are combined with the value of the Recovery Multiplier Value (bits 5-0) to control the length of recovery time after a command is active.

12. ATA MODE OPERATION

The CL-PD6729 card interfaces can be dynamically configured to support a PCMCIA-compatible ATA disk interface (commonly known as 'IDE') instead of the standard PCMCIA card interface. Disk drives that can be made mechanically-compatible with PCMCIA card dimensions can thus operate through the socket using the ATA electrical interface.

Configuring a socket to support ATA operation changes the function of certain card socket signals to support the needs of the ATA disk interface. Table 12-1 lists each interface pin and its function when a CL-PD6729 card socket is operating in ATA mode.

All register functions of the CL-PD6729 are available in ATA mode, including socket power control, interface signal disabling, and card window control. No memory operations are allowed in ATA mode.

Table 12-1. ATA Pin Cross-Reference

PCMCIA Socket Pin Number	PCMCIA Card Interface Function	ATA Interface Function
1	Ground	Ground
2	D3	D3
3	D4	D4
4	D5	D5
5	D6	D6
6	D7	D7
7	-CE1	CS0*
8	A10	n/c
9	-OE	Always low
10	A11	n/c
11	A9	CS1*
12	A8	n/c
13	A13	n/c
14	A14	n/c
15	-WE	n/c
16	-IREQ	IREQ
17	VCC	VCC
18	VPP1	n/c
19	A16	n/c
20	A15	n/c
21	A12	n/c

PCMCIA Socket Pin Number	PCMCIA Card Interface Function	ATA Interface Function
35	Ground	Ground
36	-CD1	-CD1
37	D11	D11
38	D12	D12
39	D13	D13
40	D14	D14
41	D15	D15
42	-CE2	CS1*
43	VS1	VS1
44	-IORD	-IORD
45	-IOWR	-IOWR
46	A17	n/c
47	A18	n/c
48	A19	n/c
49	A20	n/c
50	A21	n/c
51	VCC	VCC
52	VPP2	n/c
53	A22	n/c
54	A23	VU
55	A24	M/S*

Table 12-1. ATA Pin Cross-Reference *(cont.)*

PCMCIA Socket Pin Number	PCMCIA Card Interface Function	ATA Interface Function
22	A7	n/c
23	A6	n/c
24	A5	n/c
25	A4	n/c
26	A3	n/c
27	A2	A2
28	A1	A1
29	A0	A0
30	D0	D0
31	D1	D1
32	D2	D2
33	-IOIS16	-IOIS16
34	Ground	Ground

PCMCIA Socket Pin Number	PCMCIA Card Interface Function	ATA Interface Function
56	A25	CSEL
57	VS2	VS2
58	RESET	RESET*
59	-WAIT	IOCHRDY
60	-INPACK	DREQ [a]
61	-REG	DACK* [a]
62	-SPKR	LED*
63	-STSCHG	PDIAG* [a]
64	D8	D8
65	D9	D9
66	D10	D10
67	-CD2	-CD2
68	Ground	Ground

[a] Not supported by the CL-PD6729.

13. ELECTRICAL SPECIFICATIONS

13.1 Absolute Maximum Ratings

Description	Absolute Maximum Rating
Ambient temperature under bias	0°C to 70°C
Storage temperature	–65°C to 150°C
Voltage on any pin (with respect to ground)	–0.3 volts to 0.3 volts greater than voltage of the +5V pin, respective to ground
Operating power dissipation	500 mW
Power dissipation during Suspend mode	10 mW
Power supply voltage[a]	7 volts
Injection current (latch up)[a]	25 mA

[a] Stresses above those listed may cause permanent damage to system components. These are stress ratings only; functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect system reliability.

13.2 DC Specifications

Table 13-1. General DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
C_{IN}	Input capacitance		10.0	pF	
C_{OUT}	Output capacitance		10.0	pF	
I_{IL}	Input leakage	–10.0	10.0	µA	$0 < V_{IN} <$ respective V_{CC} supply pin
I_{PU}	Internal pull-up current	–30	–400	µA	

Table 13-2. PCMCIA Bus Interface DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
$SOCKET\_VCC_{5V}$	Power supply voltage	4.5	5.5	V	Normal operation
$SOCKET\_VCC_{3V}$		3.0	3.6	V	
V_{IH}	Input high voltage	2.0		V	V_{DD} core voltage = 3.0V, **Misc Control 2** register, bit 3 = '0'
		2.0		V	V_{DD} core voltage = 4.5V, **Misc Control 2** register, bit 3 = '1'
V_{IL}	Input low voltage		0.8	V	V_{DD} core voltage = 3.6V, **Misc Control 2** register, bit 3 = '0'
			0.8	V	V_{DD} core voltage = 5.5V, **Misc Control 2** register, bit 3 = '1'
V_{IHC}	Input high voltage CMOS	$0.7\ V_{DD}$		V	V_{DD} core voltage = 4.5V, **Misc Control 2** register, bit 3 = '0'
V_{ILC}	Input low voltage CMOS		$0.2\ V_{DD}$	V	V_{DD} core voltage = 5.5V, **Misc Control 2** register, bit 3 = '0'
V_{OH}	Output high voltage	2.4		V	At rated I_{OH}, respective SOCKET_VCC = 3.0V
V_{OHC}	Output high voltage CMOS	SOCKET_VCC – 0.5		V	At rated I_{OHC}, respective SOCKET_VCC = 3.0V
V_{OL}	Output low voltage		0.4	V	At rated I_{OL}
I_{OH}	Output high current	–2		mA	Respective SOCKET_VCC = 3.0V, V_{OH} = 2.4V
I_{OHC}	Output high current CMOS	–1		mA	Respective SOCKET_VCC = 3.0V, V_{OHC} = SOCKET_VCC – 0.5V
I_{OL}	Output low current	2		mA	Respective SOCKET_VCC = 3.0V, V_{OL} = 0.4V

Table 13-3. PCI Bus Interface DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
PCI_VCC_{5V}	Power supply voltage	4.5	5.5	V	Normal operation
PCI_VCC_{3V}		3.0	3.6	V	
V_{IH}[a]	Input high voltage	2.0		V	V_{DD} core voltage = 3.0V
V_{IL}[a]	Input low voltage		0.8	V	V_{DD} core voltage = 3.6V
V_{IHC}[a]	Input high voltage CMOS	$0.7\ V_{DD}$[b]		V	V_{DD} core voltage = 4.5V
V_{ILC}[a]	Input low voltage CMOS		$0.2\ V_{DD}$[b]	V	V_{DD} core voltage = 5.5V
V_{OH}	Output high voltage	2.4		V	At rated I_{OH}, PCI_VCC = 3.0V
V_{OHC}	Output high voltage CMOS	PCI_VCC – 0.5		V	At rated I_{OHC}, PCI_VCC = 3.0V
V_{OL}	Output low voltage		0.5	V	At rated I_{OL}
I_{OH}	Output current high	–5		mA	PCI_VCC = 3.0V, V_{OH} = 2.4V
I_{OHC}	Output current high CMOS	–1		mA	PCI_VCC = 3.0V, V_{OHC} = PCI_VCC – 0.5V
I_{OL}	Output current low	16		mA	PCI_VCC = 3.0V, V_{OL} = 0.5V

[a] When CORE_VDD is 3.3V, input thresholds are TTL-compatible; when CORE_VDD is 5V, input thresholds are CMOS-compatible.

[b] The value of the input threshold level is dependent on the voltage applied to the CORE_VDD pin of the CL-PD6729.

Table 13-4. Power Control Interface (+5V Powered) DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
+5V	+5V supply voltage	Highest V_{CC} – 0.3	5.5	V	
V_{IH}	Input high voltage	2.0		V	+5V pin voltage = 4.5V
V_{IL}	Input low voltage		0.8	V	+5V pin voltage = 5.5V
V_{OH}	Output high voltage	2.4		V	+5V pin voltage = 4.5V, I_{OH} = –5 mA
V_{OHC}	Output high voltage CMOS	+5V voltage – 0.5		V	+5V pin voltage = 4.5V, I_{OH} = –1 mA
V_{OL}	Output low voltage		0.4	V	
I_{OH}	Output current high	–5		mA	Respective +5V pin voltage = 4.5V, V_{OH} = 2.4V
I_{OHC}	Output current high CMOS	–1		mA	Respective +5V pin voltage = 4.5V, V_{OHC} = +5V pin voltage – 0.5V
I_{OL}	Output current low	16		mA	Respective +5V pin voltage = 4.5V, V_{OL} = 0.4V

Table 13-5. Operating Current Specifications (3.3V)

Symbol	Parameter	MIN	TYP	MAX	Unit	Conditions
$Icc_{tot(1)}$	Power supply current, operating	<6	8	>20	mA	CORE_VDD = 3.3V; +5V, SOCKET_VCC, and PCI_VCC = 5.0V
$Icc_{tot(2)}$	Power supply current, Suspend mode (**Misc Control 2**, bit 2 = '1')		6		mA	CORE_VDD = 3.3V; +5V, SOCKET_VCC, and PCI_VCC = 5.0V
$Icc_{tot(3)}$	Power supply current, RST# active, no clocks		<250		µA	CORE_VDD = 3.3V; +5V, SOCKET_VCC, and PCI_VCC = 5.0V

Table 13-6. Operating Current Specifications (5.0V)

Symbol	Parameter	MIN	TYP	MAX	Unit	Conditions
$Icc_{tot(1)}$	Power supply current, operating	<8	12	>20	mA	CORE_VDD, +5V, SOCKET_VCC, and PCI_VCC = 5.0V
$Icc_{tot(2)}$	Power supply current, Suspend mode (**Misc Control 2**, bit 2 = '1')		2.5		mA	CORE_VDD, +5V, SOCKET_VCC, and PCI_VCC = 5.0V
$Icc_{tot(3)}$	Power supply current, RST# active, no clocks		<250		µA	CORE_VDD, +5V, SOCKET_VCC, and PCI_VCC = 5.0V

13.3 AC Timing Specifications

This section includes system timing requirements for the CL-PD6729. Unless otherwise specified, timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0°C to 70°C, and V_{CC} varying from 3.0V to 3.6V or 4.5V to 5.5V DC. The PCI bus speed is 33 MHz unless otherwise specified. Note the following conventions:

- A pound sign (#) at the end of a pin name indicates an active-low signal for the PCI bus.
- A dash (-) at the beginning of a pin name indicates an active-low signal for the PCMCIA bus.
- An asterisk (*) at the end of a pin name indicates an active-low signal that is a general-interface for the CL-PD6729.

Additionally, the following statements are true for all timing information:

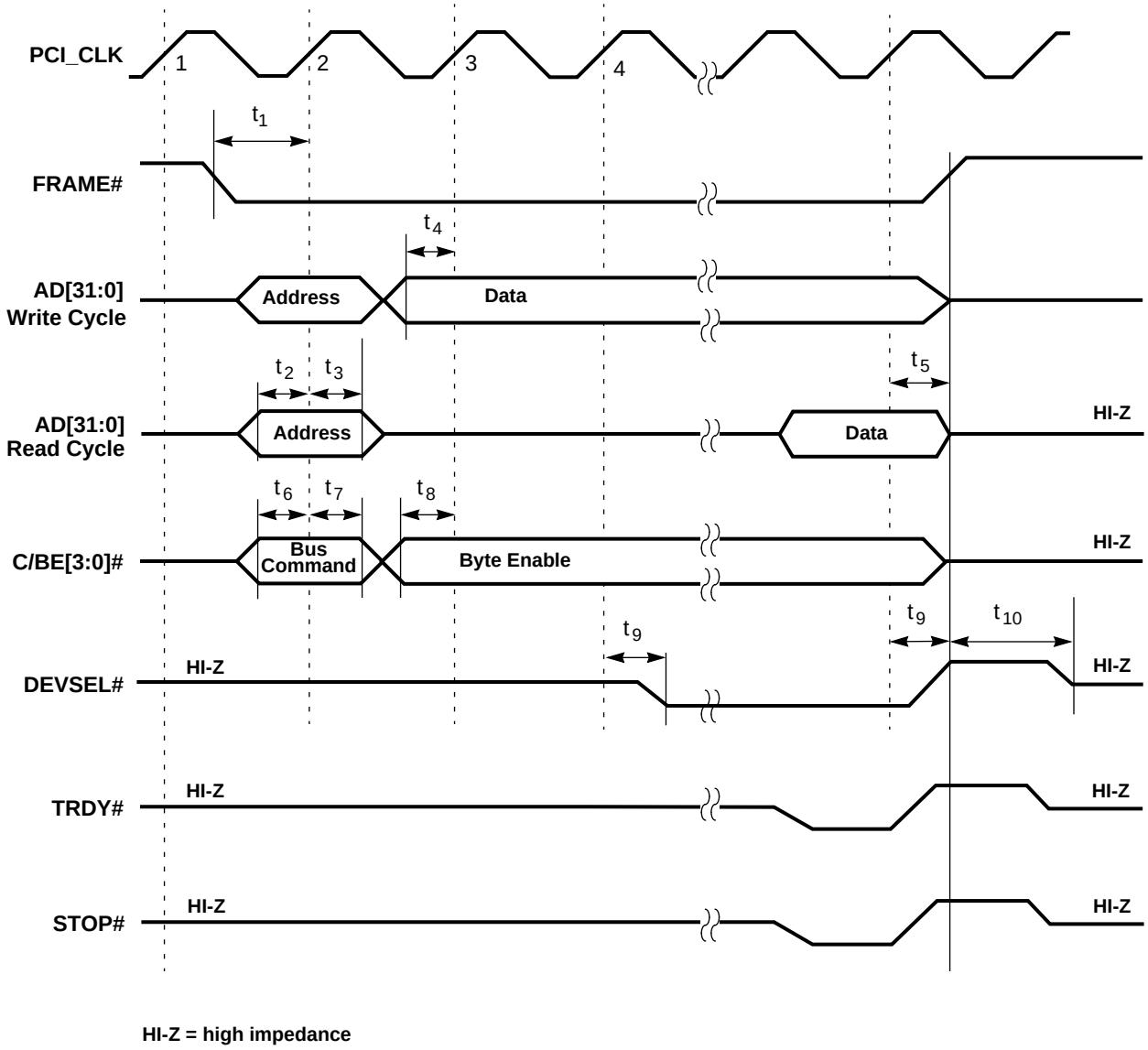
- All timings assume a load of 50 pF.
- TTL signals are measured at TTL threshold; CMOS signals are measured at CMOS threshold.

Table 13-7. Index of AC Timing Specifications

13.3.1 PCI Bus Timing

Table 13-8. FRAME#, AD[31:0], C/BE[3:0]#, and DEVSEL#

Symbol	Parameter	PCI_VCC = 3.3 V		PCI_VCC = 5.0 V		Units
		MIN	MAX	MIN	MAX	
t_1	FRAME# setup to PCI_CLK	7	–	7	–	ns
t_2	AD[31:0] (address) setup to PCI_CLK	7	–	7	–	ns
t_3	AD[31:0] (address) hold from PCI_CLK	0	–	0	–	ns
t_4	AD[31:0] (data) setup to PCI_CLK	7	–	7	–	ns
t_5	AD[31:0] (data) active to HI-Z from PCI_CLK	0	28	0	28	ns
t_6	C/BE[3:0]# (bus command) setup to PCI_CLK	7	–	7	–	ns
t_7	C/BE[3:0]# (bus command) hold from PCI_CLK	0	–	0	–	ns
t_8	C/BE[3:0]# (byte enable) setup to PCI_CLK	7	–	7	–	ns
t_9	DEVSEL# delay from PCI_CLK	–	11	–	11	ns
t_{10}	DEVSEL# high before HI-Z	1	–	1	–	PCI_CLK



HI-Z = high impedance

Figure 13-1. FRAME#, AD[31:0], C/BE[3:0]#, and DEVSEL# (PCI™ Bus)

Table 13-9. TRDY# and STOP# Delay

Symbol	Parameter	PCI_VCC = 3.3 V		PCI_VCC = 5.0 V		Units
		MIN	MAX	MIN	MAX	
t_1	TRDY# active delay from PCI_CLK	–	11	–	11	ns
t_2	TRDY# inactive delay from PCI_CLK	–	11	–	11	ns
t_3	TRDY# high before HI-Z	1	–	1	–	PCI_CLK
t_4	STOP# active delay from PCI_CLK	–	11	–	11	ns
t_5	STOP# inactive delay from PCI_CLK	–	11	–	11	ns
t_6	STOP# high before HI-Z	1	–	1	–	PCI_CLK

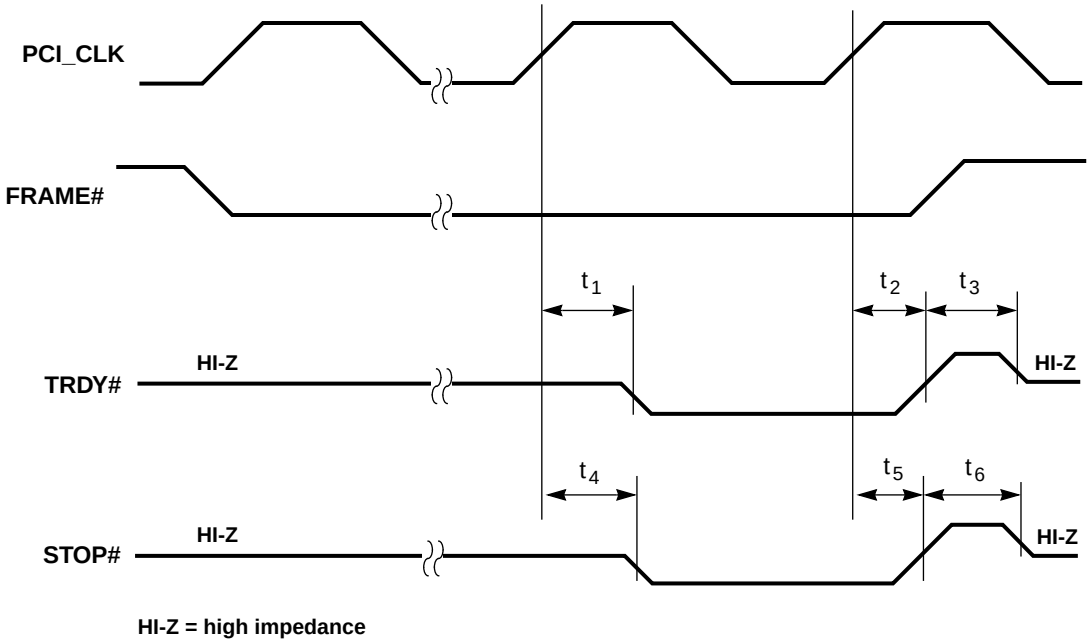


Figure 13-2. TRDY# and STOP# Delay (PCI™ Bus)

Table 13-10. IDSEL Timing in a Configuration Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	IDSEL setup to PCI_CLK	7	–	ns
t_2	IDSEL hold from PCI_CLK	0	–	ns

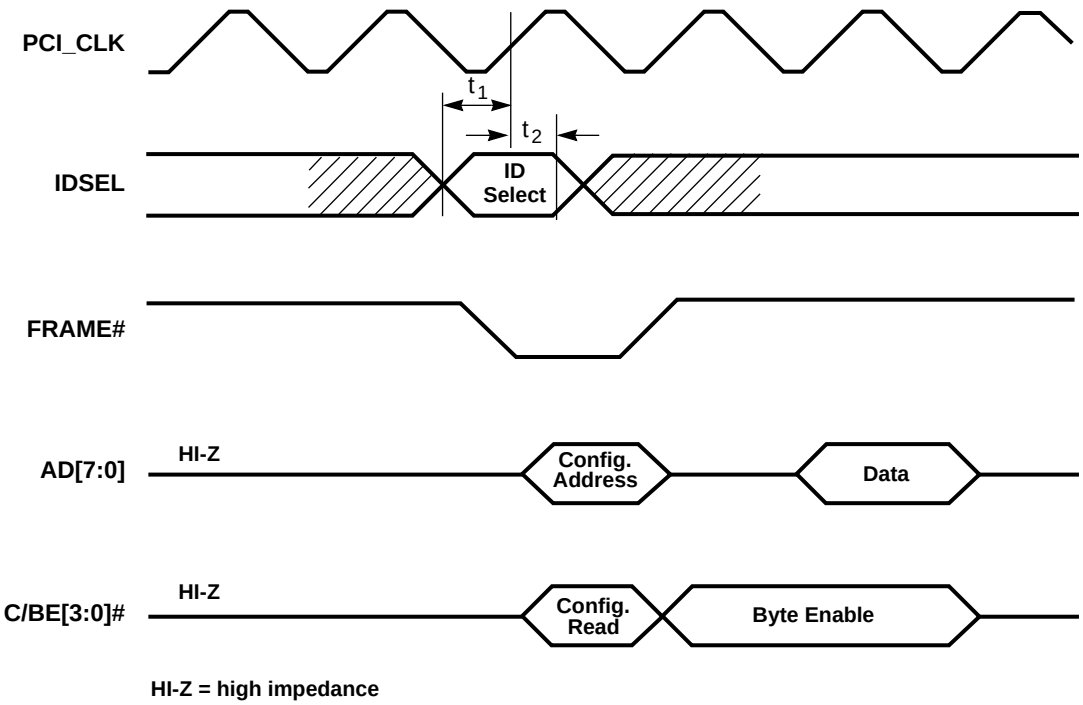
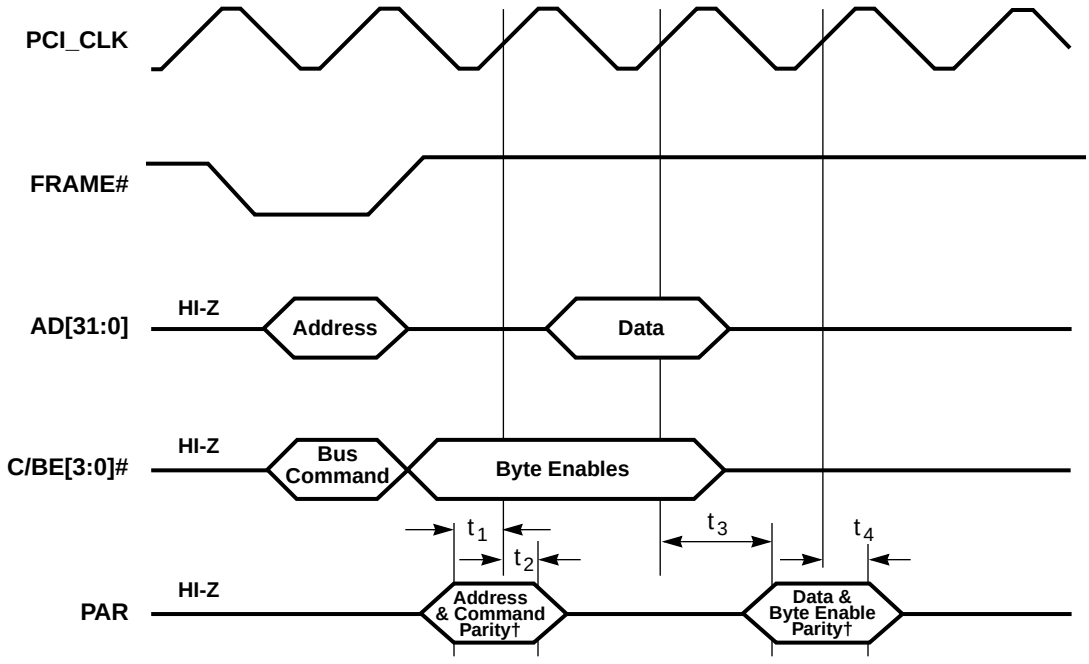


Figure 13-3. IDSEL Timing in a Configuration Cycle (PCI™ Bus)

Table 13-11. PAR Timing

Symbol	Parameter	MIN	MAX	Units
t_1	PAR setup to PCI_CLK (input to CL-PD6729)	7	–	ns
t_2	PAR hold from PCI_CLK (input to CL-PD6729)	0	–	ns
t_3	PAR valid delay from PCI_CLK (output from CL-PD6729)	–	11	ns
t_4	PAR hold from PCI_CLK (output from CL-PD6729)	0	–	ns



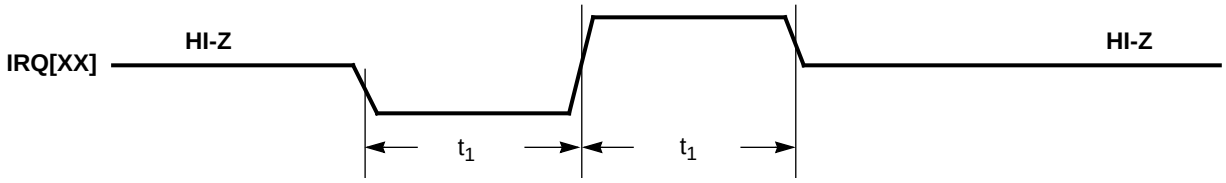
HI-Z = high impedance

† PAR goes high or low depending on AD[31:0] and C/BE[3:0]# values.

13.3.2 System Interrupt Timing

Table 13-12. Pulse Mode Interrupt Timing

Symbol	Parameter	MIN	MAX	Units
t_1	IRQ[XX] low or high	4	4	PCI_CLK



HI-Z = high impedance
NOTE: Each time indicated is 4 PCI clocks or 4 external clocks.

Figure 13-5. Pulse Mode Interrupt Timing

13.3.3 PCMCIA Bus Timing Calculations

Calculations for minimum PCMCIA cycle Setup, Command, and Recovery timings are made by first calculating factors derived from the applicable timer set's timing registers and then by applying the factor to an equation relating it to the internal clock period.

The PCMCIA cycle timing factors, in terms of the number of internal clocks, are calculated as follows:

$$S = (N_{pres} \times N_{val}) + 1$$

$$C = (N_{pres} \times N_{val}) + 1$$

$$R = (N_{pres} \times N_{val}) + 1$$

N_{pres} and N_{val} are the specific selected prescalar and multiplier value from the timer set's Setup, Command, and Recovery Timing registers (see Chapter 11 for description of these registers).

From this, a PCMCIA cycle's Setup, Command, and Recovery time for the selected timer set are calculated as follows:

$$\text{Minimum Setup time} = (S \times Tcp) - 20\ ns$$

$$\text{Minimum Command time} = (C \times Tcp) - 20\ ns$$

$$\text{Minimum Recovery time} = (R \times Tcp) - 20\ ns$$

Tcp is two times the period of the PCI bus clock connected to the CL-PD6729 PCI_CLK pin.

If PCI_CLK operates at 33 MHz, then:

$$Tcp = 60\ ns$$

The timing diagrams that follow were derived for a CL-PD6729 using the PCI clock at 33 MHz. The examples are for the default values of the Timing registers for Timer Set 0, as follows:

Timing Register Name (Timer Set 0)	Index	Value (Default)	Resultant N_{pres}	Resultant N_{val}
Setup Timing 0	3Ah	01h	1	1
Command Timing 0	3Bh	05h	1	5
Recovery Timing 0	3Ch	00h	1	0

Thus the minimum times for the default values are as follows:

$$\text{Minimum Setup time} = (S \times Tcp) - 20\ ns = \{[(1 \times 1) + 1] \times 60\ ns\} - 20\ ns = \mathbf{100\ ns}$$

$$\text{Minimum Command time} = (C \times Tcp) - 20\ ns = \{[(1 \times 5) + 1] \times 60\ ns\} - 20\ ns = \mathbf{340\ ns}$$

$$\text{Minimum Recovery time} = (R \times Tcp) - 20\ ns = \{[(1 \times 0) + 1] \times 60\ ns\} - 30\ ns = \mathbf{30\ ns}$$

13.3.4 PCMCIA Bus Timing

Table 13-13. Memory Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	-REG, -CE[2:1], Address, and Write Data setup to Command active[1]	(S × Tcp) – 20		ns
t_2	Command pulse width[2]	(C × Tcp) – 20		ns
t_3	Address hold and Write Data valid from Command inactive[3]	(R × Tcp) – 30		ns
t_4	-WAIT active from Command active		(C – 2)Tcp – 30	ns
t_5	Command hold from -WAIT inactive	2 Tcp		ns
t_6	Data setup before -OE inactive	(2 Tcp) + 20		ns
t_7	Data hold after -OE inactive	0		ns
t_8	Data valid from -WAIT inactive		Tcp + 20	ns

1 The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 100 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 92.

2 The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 340 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 92.

3 The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 92.

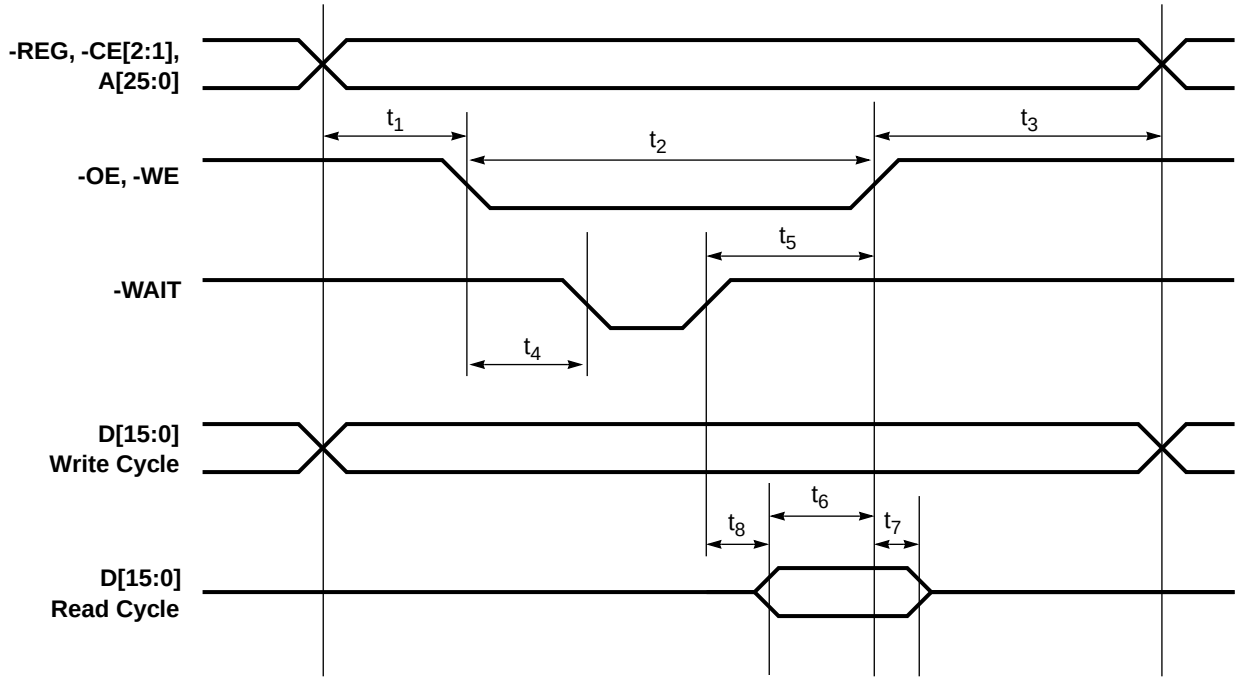


Figure 13-6. Memory Read/Write Timing

Table 13-14. Word I/O Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	-REG or Address setup to Command active[1]	(S × Tcp) – 20		ns
t_2	Command pulse width[2]	(C × Tcp) – 20		ns
t_3	Address hold and Write Data valid from Command inactive[3]	(R × Tcp) – 20		ns
t_4	-WAIT active from Command active[4]		(C – 2) Tcp – 30	ns
t_5	Command hold from -WAIT inactive	(2 Tcp) + 20		
t_{ref}	Card -IOIS16 delay from valid Address (PCMCIA card specification)		35	ns
t_6	-IOIS16 setup time before Command end	(3 Tcp) + 20		ns
t_7	-CE2 delay from -IOIS16 active[4]	Tcp – 20		ns
t_8	Data valid from -WAIT inactive		Tcp + 20	ns
t_9	Data setup before -IORD inactive	(2 Tcp) + 20		ns
t_7	Data hold after -IORD inactive	0		ns

[1] The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 100 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 92.

[2] The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 340 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 92.

[3] The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 92.

[4] For typical active timing programmed at 340 ns, maximum -WAIT timing is 200 ns after Command active.

[5] -IOIS16 must go low within 3Tcp + 20 ns of the cycle beginning or -IOIS16 will be ignored and -CE will not be activated.

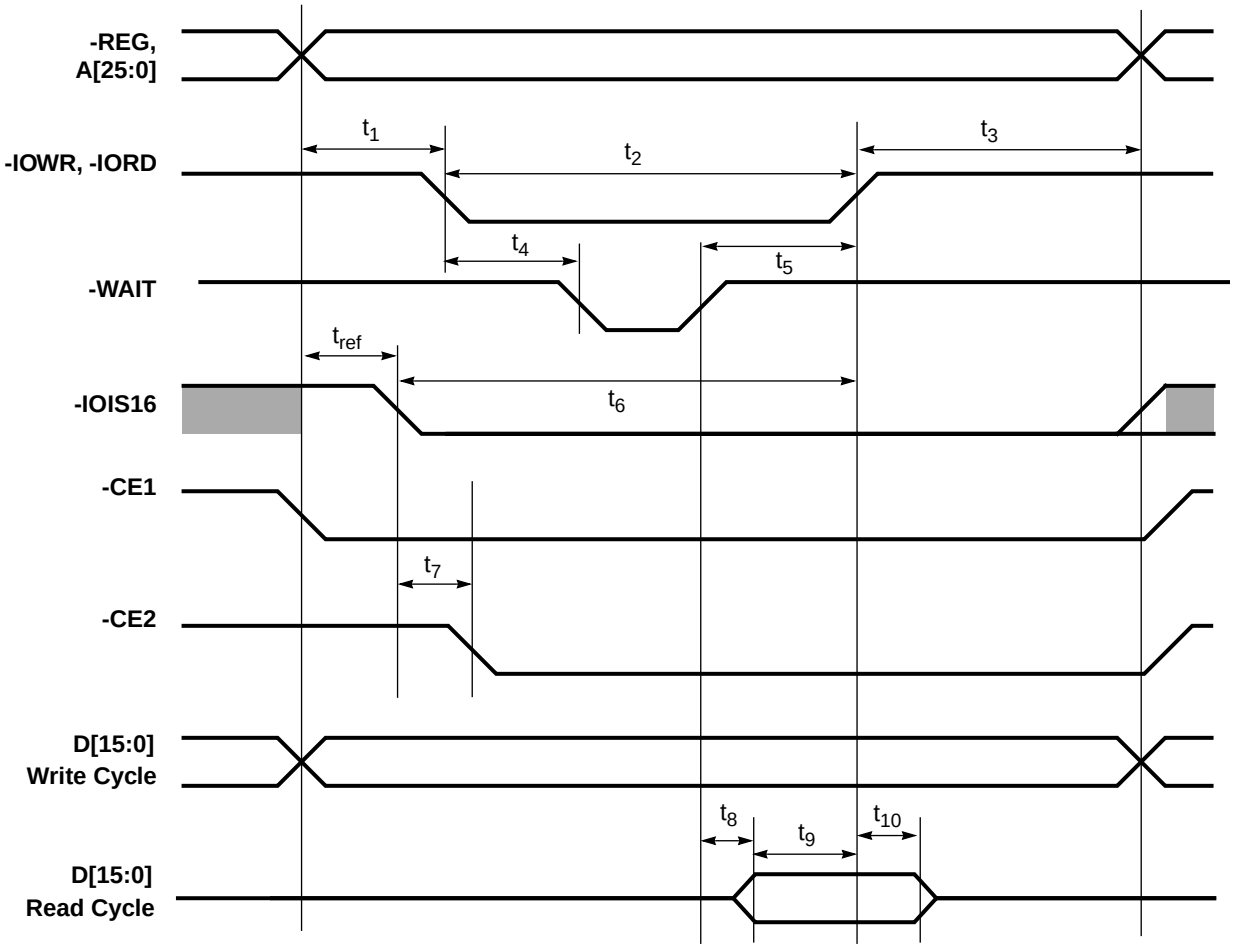


Figure 13-7. Word I/O Read/Write Timing

Table 13-15. PCMCIA Read/Write Timing when System is 8-Bit

Symbol	Parameter	MIN	MAX	Units
t_1	-REG or Address setup to Command active[1]	(S × Tcp) – 10		ns
t_2	Command pulse width[2]	(C × Tcp) – 10		ns
t_3	Address hold from Command inactive[3]	(R × Tcp) – 10		ns
t_4	Data setup before Command inactive	(2 Tcp) + 10		ns
t_5	Data hold after command inactive	0		ns

1 The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 100 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 92.

2 The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 340 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 92.

3 The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 92.

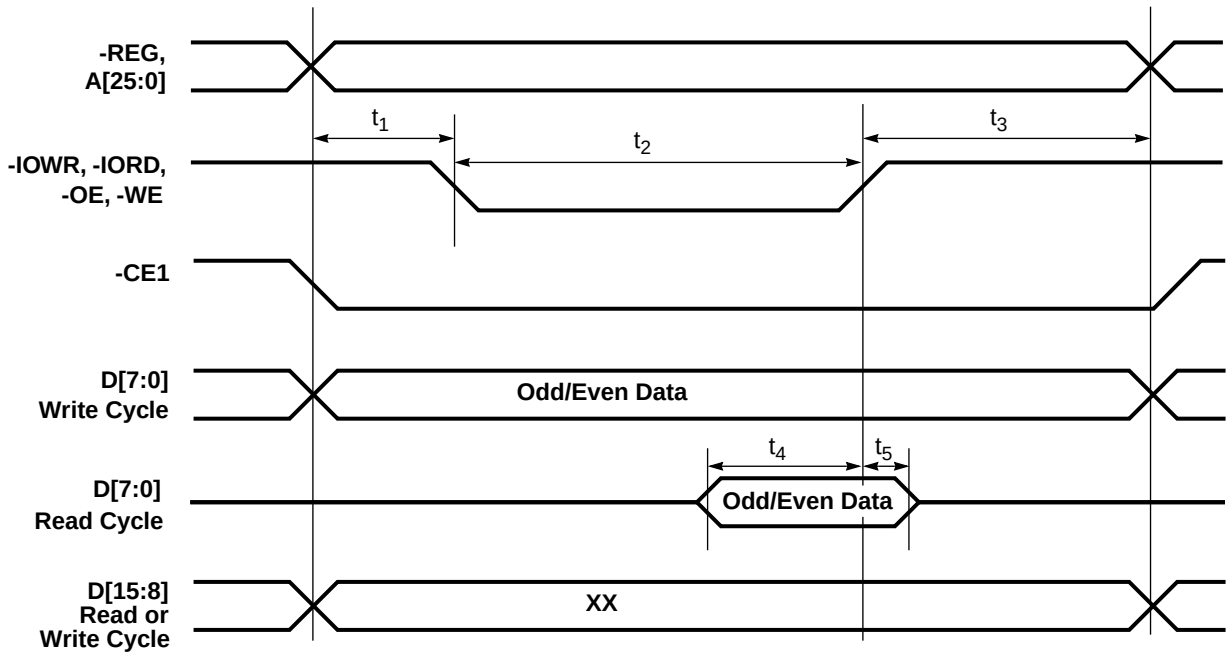


Figure 13-8. PCMCIA Read/Write Timing when System is 8 Bit ($\overline{SBHE}$ Tied High)

Table 13-16. Normal Byte Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Address setup to Command active[1]	(S × Tcp) – 20		ns
t_2	Command pulse width[2]	(C × Tcp) – 20		ns
t_3	Address hold from Command inactive[3]	(R × Tcp) – 20		ns

1 The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 100 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 92.

2 The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 340 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 92.

3 The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 92.

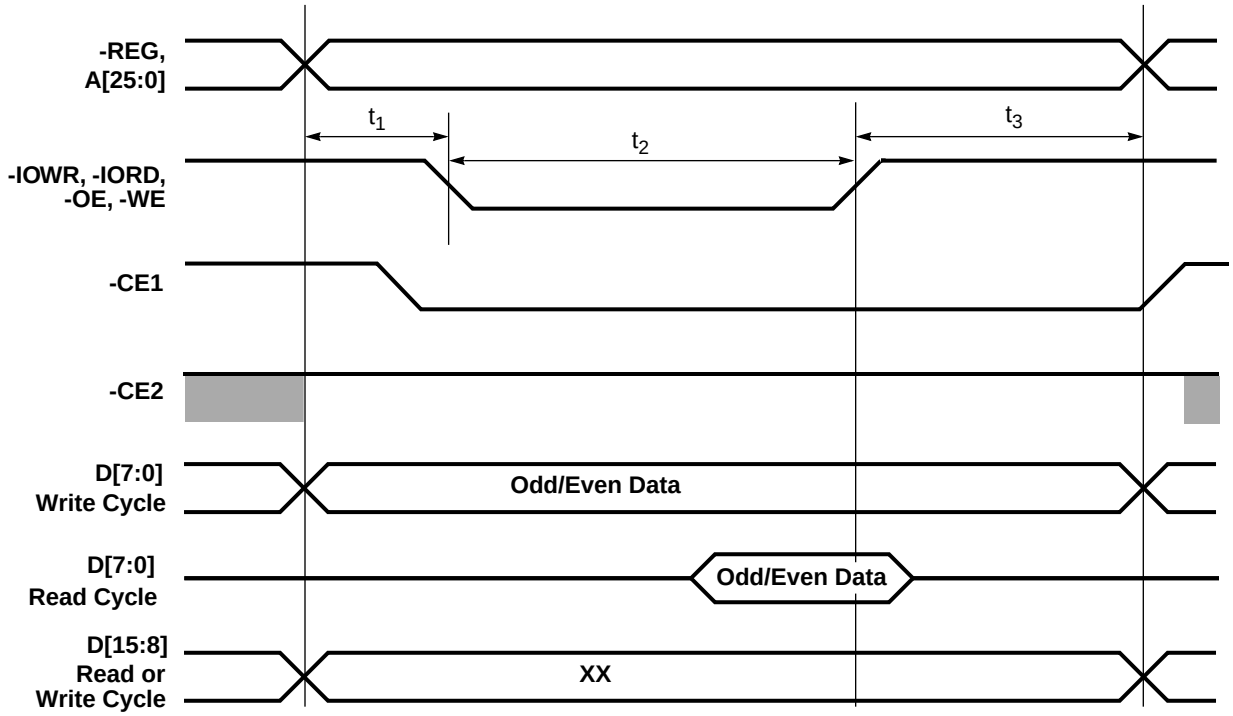


Figure 13-9. Normal Byte Read/Write Timing (that is, all other byte accesses, including odd I/O cycles where -IOIS16 is low)

Table 13-17. 16-Bit System to 8-Bit I/O Card: Odd Byte Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Address change to -IOIS16 inactive[4]		(3Tcp) + 20	ns
t_2	-IOIS16 inactive to -CE2 inactive		20	ns
t_3	-IOIS16 inactive to -CE1 active		20	ns
t_4	Address setup to Command active[1]	(S × Tcp) – 20		ns
t_5	Command pulse width[2]	(C × Tcp) – 20		ns
t_6	Address hold from Command inactive[3]	(R × Tcp) – 20		ns

1 The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 100 ns. S = ($N_{pres} \times N_{val}$ + 1), see page 92.

2 The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 340 ns. C = ($N_{pres} \times N_{val}$ + 1), see page 92.

3 The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. R = ($N_{pres} \times N_{val}$ + 1), see page 92.

4 -IOIS16 level from card must be valid within 3 clocks of an address change to the card.

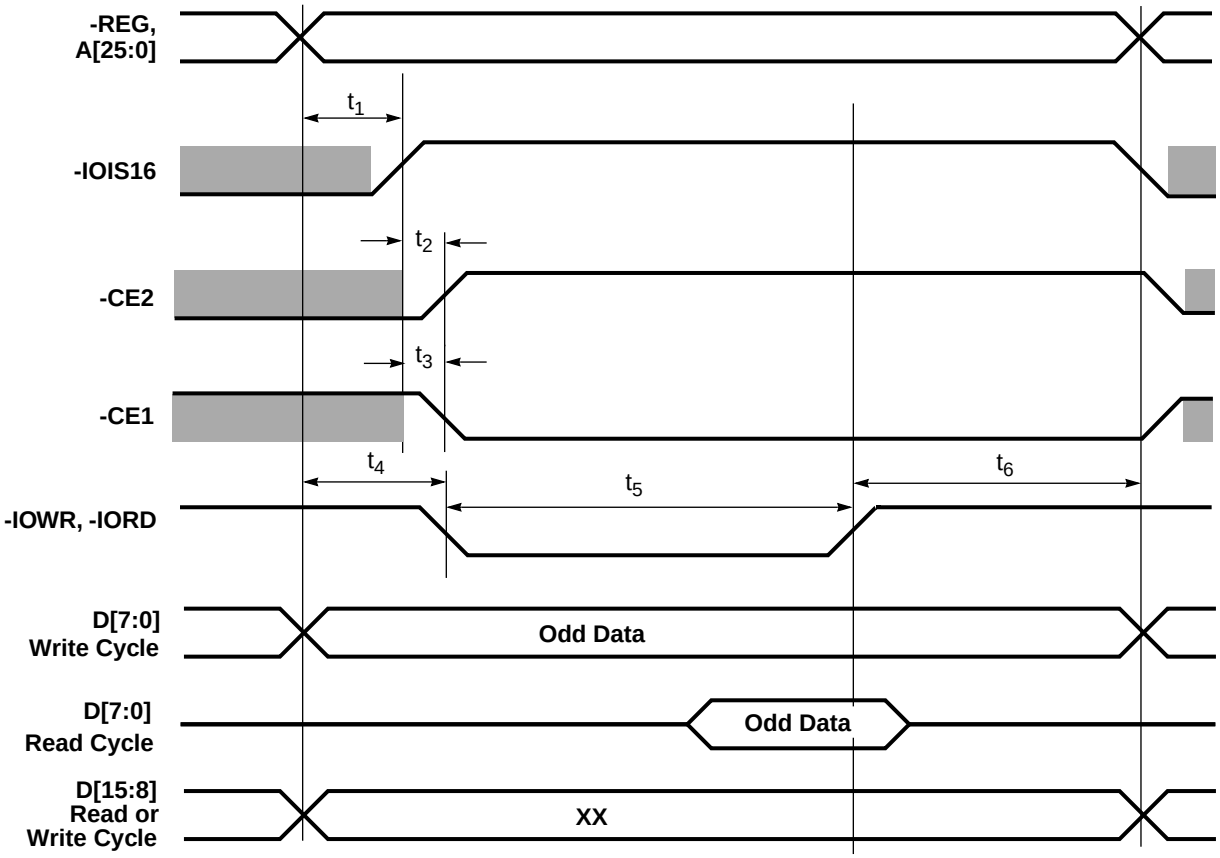
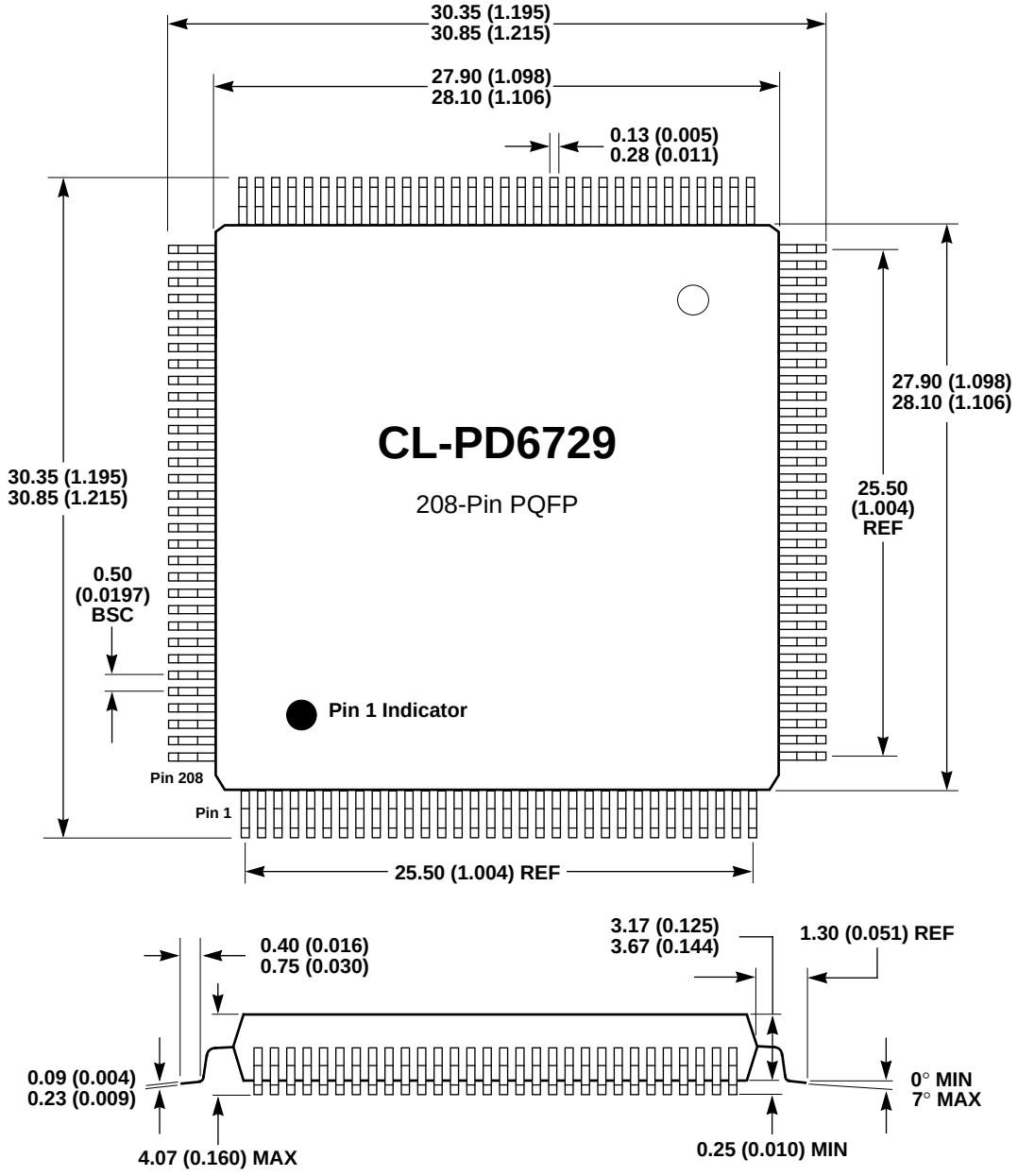


Figure 13-10. 16-Bit System to 8-Bit I/O Card: Odd Byte Timing

14. PACKAGE DIMENSIONS

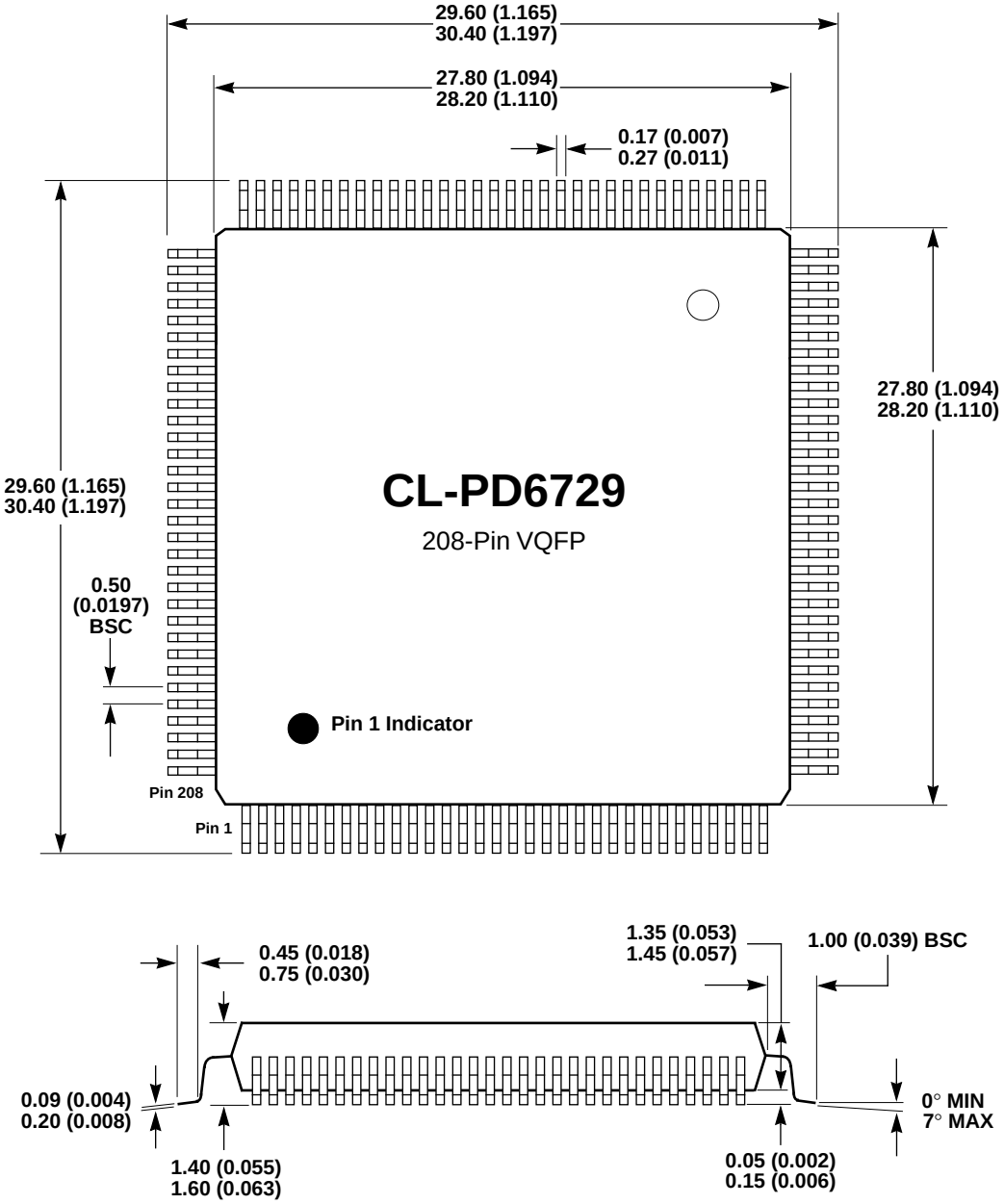
14.1 208-Pin PQFP Package Outline Drawing



NOTES:

1) Dimensions are in millimeters (inches), and the controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

14.2 208-Pin VQFP Package Outline Drawing

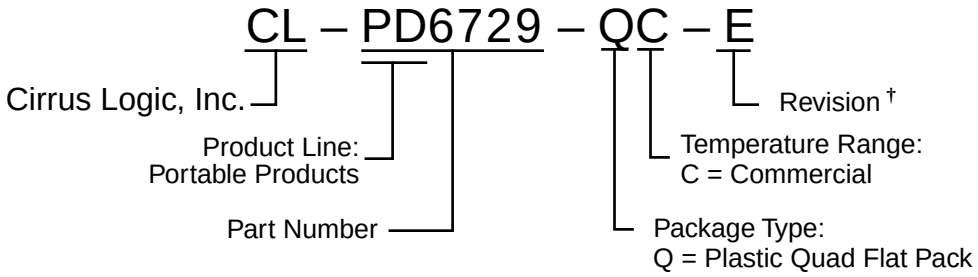


NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

15. ORDERING INFORMATION

The order number for the part is:



† Contact Cirrus Logic for up-to-date information on revisions.

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