O₂Micro
Breathing Life into Computing

OZ6833
Saturn ACPI CardBus Controller

Features

- **Single-chip CardBus host adapter**
- **Supports 2 PCMCIA 2.1 and JEIDA 4.2 R2 cards or 2 CardBus cards**
- **Supports multiple FIFOs for PCI/CB data transfer**
- **Supports up to 33 MHz clock to CardBus cards**
- **Compliant with PCI spec. V2.1S , 1995 PC Card Standard and JEIDA 4.1**
- **ACPI-PCI Bus Power management Interface Specification Rev1.0 Compliant**
- **OZ6832/CL6832 pin compatible**
- **Yenta™ -PCI to PCMCIA CardBus Bridge register compatible**
- **Programmable interrupt protocol : PCI, PCI/Way, or PC/PCI interrupt signaling modes**
- **Parallel or Serial interface to socket power control devices**
- **Zoomed Video Support**
- **3V card protection during host system suspend mode with Auto Card VS# re-sensing**
- **Socket-to-socket transfer (bus master) capability**
- **Supports both 5V and 3.3V PC cards**
- **Supports PCMCIA_ATA Specification**
- **Supports Direct Memory Access for PC/PCI and PC/Way on Both PC Card sockets**
- **No buffers required for PC Card socket interface**
- **Win'97 IRQ and PC-97compliant**
- **PC 98 -Subsystem Vendor ID support.**

Ordering Information

OZ6833T - 208pin TQFP

Description

The OZ6833 Saturn ACPI CardBus controller provides a high performance, synchronous, 32-bit, bus master/target interface between computers and plug in PC Cards. CardBus is the new 32-bit interface standard of Personal Computer Memory Card International Association, PCMCIA. The CardBus provides 32-bit interface with multiplexed address and data lines. This will allow the addition of high performance computer system enhancements and new functions in a user-friendly way. Further, the expansion capability of the CardBus will provide benefits to the end user. CardBus is intended to support "temporal" add-in functions on PC Cards, such as Memory cards, Network interfaces, FAX/Modems and other wireless communication cards, etc. The high performance

and capability of the CardBus interface will enable the new development of many new functions and applications.

The OZ6833 CardBus controller is a 33 MHz PCI compliant master/target device which attaches to the PCI bus and manages two PC Card sockets. The PC Card sockets will support both 3.3v/5v of either 8/16-bit PCMCIA R2 card or 32-bit CardBus card. The support for the R2 card is compatible to an Intel 82365SL PCIC controller, and the support for the CardBus card is fully compatible to 1995 PC Card Standard CardBus specification. The OZ6833 is a stand alone device, which means that it does not require an additional buffer chip for the two PC Card socket interface. The OZ6833 implemented FIFO data buffer for the PCI and CardBus interface to provide better PCI bus access.
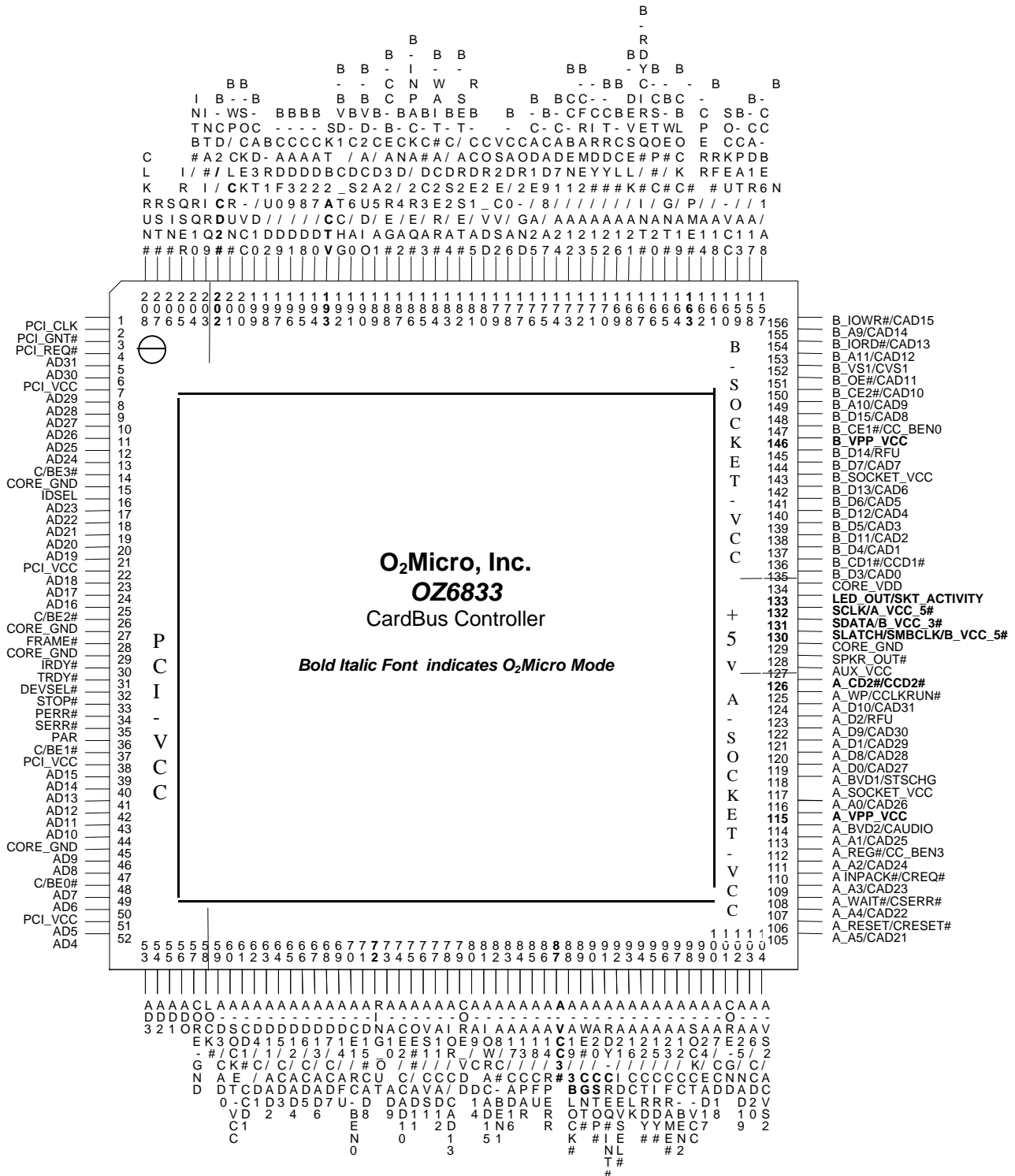
The FIFO buffers will allow the bridge to accept data from a target bus while trying to move data to it. This helps prevent deadlocks. In addition, the OZ6833 is equipped with dynamic PC Card hot insertion and removal, and auto configuration capabilities.

The OZ6833 Saturn ACPI provides mixed 5v/3.3v capability for power saving. An advanced CMOS process is utilized to minimize system power consumption. The device also provides a power-down mode to allow host software to reduce power consumption further while stopping internal clock distribution and the clocks on PC Card sockets. The OZ6833 is not only a CardBus bridge, but it is also a socket controller. The OZ6833 supports two master devices and arbitrates the priority of each. Further, the OZ6833 supports inter CardBus direct data transfer. The register set in the OZ6833 is the superset of the OZ67xx register set, assuring full compatibility with existing socket/card-services software and PC-card applications. The OZ6833 is a PCMCIA R2/CardBus controller, which provides the most advanced design flexibility for the PC Cards interface in notebook computer design.

To enhance the performance between the PCI bus and any CardBus card, 2 buffers (each composed of 16 double words) are added on both sides going from PCI to CB, or CB to PCI. By implementing these buffers, the OZ6833 will not refuse the data from a target bus while trying to move data to it and prevent deadlock situations.

In order to allow maximum flexibility for system designers, the CINT# of the PC card 32-bit could be programmed to be steered to either INTA# or INTB# of the PCI bus. Further, the interrupts may be programmed to routed through the bridge to either PCI INT lines or to IRQ interrupts on the ISA bus.

O₂Micro
2901 Tasman Drive, Ste. 205
Santa Clara, CA 95054   Page 1

Tel: (408) 987-5920
Fax: (408) 987-5929
©OZ6833-DS-1.2

Pin Diagram

O₂Micro, Inc.
OZ6833
CardBus Controller

Bold Italic Font indicates O₂Micro Mode

Left side (PCI-VCC) — pins 1–52:

Pin	Signal
1	PCI_CLK
2	PCI_GNT#
3	PCI_REQ#
4	AD31
5	AD30
6	PCI_VCC
7	AD29
8	AD28
9	AD27
10	AD26
11	AD25
12	AD24
13	C/BE3#
14	CORE_GND
15	IDSEL
16	AD23
17	AD22
18	AD21
19	AD20
20	AD19
21	PCI_VCC
22	AD18
23	AD17
24	AD16
25	C/BE2#
26	CORE_GND
27	FRAME#
28	CORE_GND
29	IRDY#
30	TRDY#
31	DEVSEL#
32	STOP#
33	PERR#
34	SERR#
35	PAR
36	C/BE1#
37	PCI_VCC
38	AD15
39	AD14
40	AD13
41	AD12
42	AD11
43	AD10
44	CORE_GND
45	AD9
46	AD8
47	C/BE0#
48	AD7
49	AD6
50	PCI_VCC
51	AD5
52	AD4

Right side (B-SOCKET-VCC / +5v A-SOCKET-VCC) — pins 105–156:

Pin	Signal
156	B_IOWR#/CAD15
155	B_A9/CAD14
154	B_IORD#/CAD13
153	B_A11/CAD12
152	B_VS1/CVS1
151	B_OE#/CAD11
150	B_CE2#/CAD10
149	B_A10/CAD9
148	B_D15/CAD8
147	B_CE1#/CC_BEN0
146	**B_VPP_VCC**
145	B_D14/RFU
144	B_D7/CAD7
143	B_SOCKET_VCC
142	B_D13/CAD6
141	B_D6/CAD5
140	B_D12/CAD4
139	B_D5/CAD3
138	B_D11/CAD2
137	B_D4/CAD1
136	B_CD1#/CCD1#
135	B_D3/CAD0
134	CORE_VDD
133	**LED_OUT/SKT_ACTIVITY**
132	**SCLK/A_VCC_5#**
131	**SDATA/B_VCC_3#**
130	**SLATCH/SMBCLK/B_VCC_5#**
129	CORE_GND
128	SPKR_OUT#
127	AUX_VCC
126	**A_CD2#/CCD2#**
125	A_WP/CCLKRUN#
124	A_D10/CAD31
123	A_D2/RFU
122	A_D9/CAD30
121	A_D1/CAD29
120	A_D8/CAD28
119	A_D0/CAD27
118	A_BVD1/STSCHG
117	A_SOCKET_VCC
116	A_A0/CAD26
115	**A_VPP_VCC**
114	A_BVD2/CAUDIO
113	A_A1/CAD25
112	A_REG#/CC_BEN3
111	A_A2/CAD24
110	A_INPACK#/CREQ#
109	A_A3/CAD23
108	A_WAIT#/CSERR#
107	A_A4/CAD22
106	A_RESET/CRESET#
105	A_A5/CAD21

System Block Diagram

The following diagram is a typical system block diagram utilizing the OZ6833 "SATURN ACPI" CardBus controller with other related chipset.
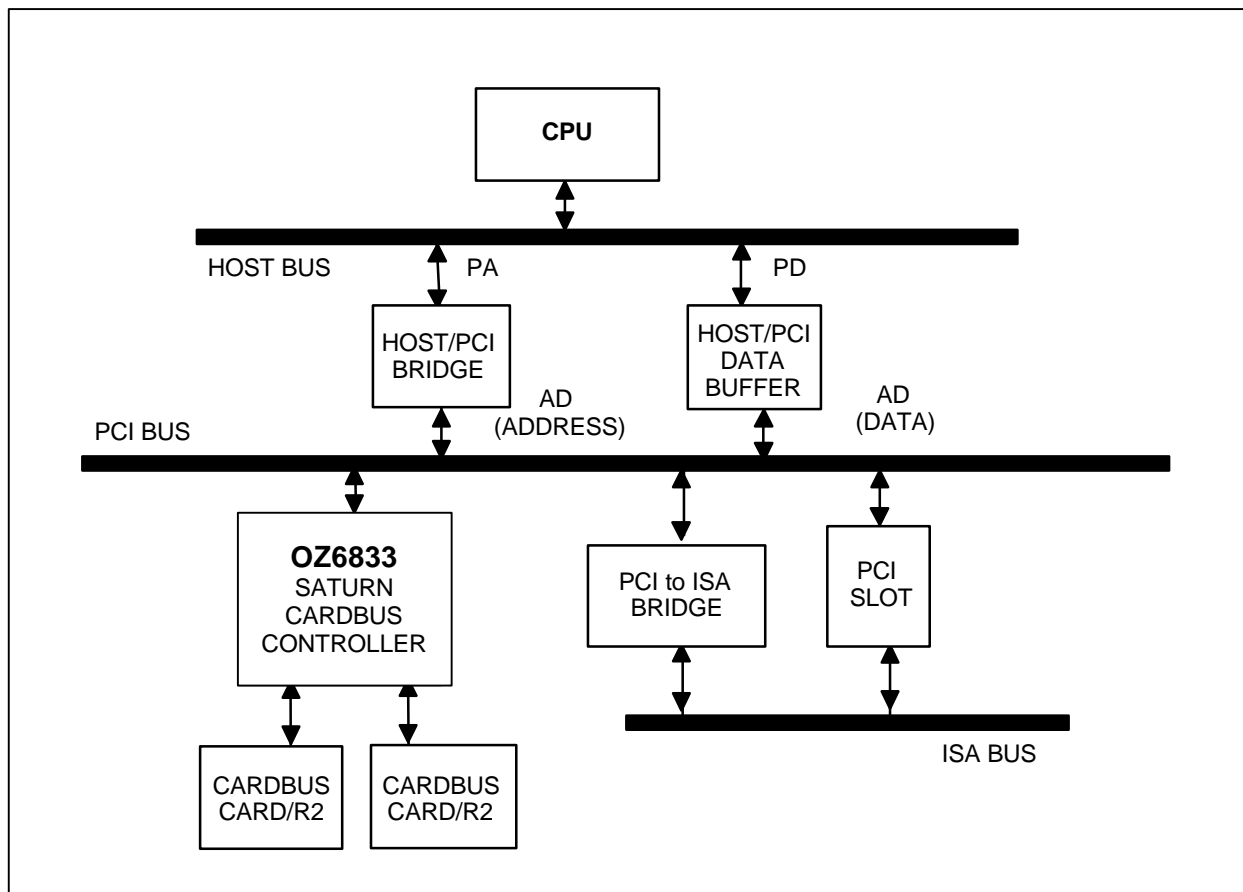
Pin List

Bold Text = Normal Default Pin Name, *Italic* = *Alternate Pin Function,* **Bold Italic =** *Alternate Pin Function is DEFAULT*

PCI Bus Interface Pins

Name	Pin No.	Type	Input	Power Rail	Drive (mA)	Definition
AD[31:0]	4-5, 7-12, 16-20, 22-24, 38-43, 45-46, 48-49, 51-56	I/O	TTL	4	PCI Spec	**PCI Bus Address Input / Data Input/ Output**
	PCI Bus Address Input / Data input/output: These pins connect to PCI bus signals AD[31:0].					
C/BE[3:0]#	13, 25, 36, 47	I/O	TTL	4	-	**PCI Bus Command / Byte Enable**
	PCI Bus Command / Byte Enable: The command signaling and byte enables are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# are interpreted as the bus commands. During the data phase, C/BE[3:0]# are interpreted as byte enables. The byte enables are to be valid for the entirety of each data phase, and they indicate which bytes in the 32-bit data path are to carry meaningful data for the current data phase.					
FRAME#	27	I/O	TTL	4	-	**Cycle Frame**
	Cycle Frame: This input indicates to the OZ6833 that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is de-asserted, the transaction is in its final phase.					
IRDY#	29	I/O	TTL	4	-	**Initiator Ready**
	Initiator Ready: This input indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#.					
TRDY#	30	I/O	TTL	4	PCI Spec	**Target Ready**
	Target Ready: This output indicates the OZ6833's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#.					
STOP#	32	I/O	TTL	4	PCI Spec	**Stop**
	Stop: This output indicates the current target is requesting the master to stop the current transaction.					
IDSEL	15	I	TTL	4	-	**Initialization Device Select**
	Initialization Device Select: This input is used as a chip select during configuration read and write transactions. This is a point-to-point signal. The OZ6833 must be connected to its own unique IDSEL line (from the PCI bus arbiter or one of the HIGH-order AD bus pins).					
DEVSEL#	31	I/O	TTL	4	PCI Spec	**Device Select**
	Device Select: The OZ6833 drives this output active (LOW) when it has decoded the PCI address as one that it is programmed to support, thereby acting as the target for the current PCI cycle.					
PERR#	33	TO	N/A	4	PCI Spec	**Parity Error**
	Parity Error: The OZ6833 drives this output active (LOW) if it detects a data parity error during a write phase.					
SERR#	34	TO	N/A	4	PCI Spec	**System Error**
	System Error: This output is pulsed by the OZ6833 to indicate an address parity error.					
PAR	35	I/O	TTL	4	PCI Spec	**Parity**
	Parity: This pin is sampled the clock cycle after completion of each corresponding address or write data phase. For read operations, this pin is driven from the cycle after TRDY# is asserted until the cycle after completion of each data phase. It ensures even parity across AD[31:0] and C/BE[3:0]#.					
PCI_CLK	1	I	TTL	4	-	**PCI Clock**
	PCI Clock: This input provides timing for all transactions on the PCI bus to and from the OZ6833. All PCI bus interface signals described in this table (Table 2-1), except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled and driven on the rising edge of PCI_CLK; and all OZ6833 PCI bus interface timing parameters are defined with respect to this edge. This input can be operated at frequencies from 0 to 33 MHz.					
RST#	207	I	TTL	1	-	**Device Reset**
	Device Reset: This input is used to initialize all registers and internal logic to their reset states and place most OZ6833 pins in a HIGH-impedance state.					
RI_OUT	72	TO	N/A	1	4mA	**Ring Indicate Out**
	Ring Indicate Out: If O$_2$ mode control register B bit 7 is a "1", as a ring indicate output from a socket's BVD1/-STSCHG/-RI input and PCI Configuration Register 90h bit[3:0]=4'b1111.					
CLKRUN#	208	I/O	TTL	4	PCI Spec	**PCI Clock Run Request**
	PCI CLK Run Request : This signal is used by the central resource to request permission to stop the PCI clock or to slow it down, and the OZ6833 responds accordingly. To enable the CLKRUN# signal, you need to enable ExCA register 3B bit[3:2].					

PME#	163	TO	N/A	5	4mA	**Power Management Event**
	Power Management Event: ACPI-PCI Bus Power Management Interface Spec, a power management event is the process by which a PCI function can request a change of its power consumption state. Typically, a device uses a PME to request a change from a power savings state to the fully operational state.					
SKTB_ACTV	193	TO	N/A	1	4mA	**Socket B Activity**
	Socket B Activity: This signal indicates that there is any activity on the socket B read/write access. Refer to PCI Configuration Register 90h					
INTA#	203	TO	N/A	4	PCI Spec	**PCI Bus Interrupt A**
	PCI Bus Interrupt A: This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the OZ6833 to the system, a common use is to connect this pin to the system PCI bus INTA# signal.					
INTB#	204	TO	N/A	4	PCI Spec	**PCI Bus Interrupt B**
	PCI Bus Interrupt B: This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the OZ6833 to the system, a common use is to connect this pin to the system PCI bus INTB# signal.					
SOUT#/ IRQSER	205	I/O	TTL	4	PCI Spec	**Interrupt Request 5 / PCI Bus Interrupt C**
	SOUT#/ IRQSER: In PC/PCI Serial Interrupt Signaling mode, this pin is the serial interrupt output, SOUT#.In PC/Way mode, this pin is the IRQ serializer pin to the interrupt controller					
SIN#	206	I/O	TTL	4	PCI Spec	**Interrupt Request 7 / PCI Bus Interrupt D**
	SIN#/:. In PC/PCI Serial Interrupt Signaling mode, this pin is the serial interrupt input, SIN#.					
GNT#	2	I	TTL	4	PCI Spec	**Grant**
	Grant : This signal indicates that access to the bus has been granted.					
REQ#	3	TO	N/A	4	PCI Spec	**Request**
	Request : This signal indicates to the arbiter that the OZ6833 requests use of the bus.					
LOCK#	58	I/O	TTL	4	PCI Spec	**PCI Lock**
	PCI LOCK# : This signal is used by a PCI master to perform a locked transaction to a target memory. LOCK# is used to prevent more than one master from using a particular system resource					
PCI_VCC	6, 21, 37, 50	PWR				
	PCI Bus VCC: These pins can be connected to either a 3.3- or 5-volt power supply. The PCI bus interface pin outputs listed in this table (Table 2-1) will operate at the voltage applied to these pins, independent of the voltage applied to other OZ6833 pin groups.					

PCMCIA Sockets Interface Pins

Socket A pin number --- Socket B pin number

Pin Name[1]	Description[2]	Pin Number		Qty.	I/O	Pwr.	Drive
		Socket A	Socket B				
-REG#/ CCBE3#	**Register Access:** During PCMCIA memory cycles, this output chooses between attribute and common memory. During I/O cycles for non-DMA transfers, this signal is active (low). During ATA mode, this signal is always inactive. For DMA cycles on the OZ6833 to a DMA-capable card, -REG is inactive during I/O cycles to indicate DACK to the PCMCIA card. In CardBus mode, this pin is the command and byte enables.	112	188	1	I/O	2 or 3	CardBus spec.
A[25:24]/ CAD[19, 17]	PCMCIA socket address 25:24 outputs. In CardBus mode, these pins are the CardBus address/data bits 19 and 17, respectively.	102, 99	176, 174	2	I/O	2 or 3	CardBus spec.
A23/ CFRAME#	PCMCIA socket address 23 output. In CardBus mode, this pin is the CardBus FRAME# signal.	96	172	1	I/O	2 or 3	CardBus spec.
A22/ CTRDY#	PCMCIA socket address 22 output. In CardBus mode, this pin is the CardBus TRDY# signal.	94	170	1	I/O-PU	2 or 3	CardBus spec.
A21/ CDEVSEL#	PCMCIA socket address 21 output. In CardBus mode, this pin is the CardBus DEVSEL# signal.	92	168	1	I/O-PU	2 or 3	CardBus spec.
A20/ CSTOP#	PCMCIA socket address 20 output. In CardBus mode, this pin is the CardBus STOP# signal	90	166	1	I/O-PU	2 or 3	CardBus spec.
A19/ CBLOCK#	PCMCIA socket address 19 output. In CardBus mode, this signal is the CardBus LOCK# signal used for locked transactions.	88	164	1	I/O-PU	2 or 3	CardBus spec.
A18/ RFU	PCMCIA socket address 18 output. In CardBus mode, this pin is reserved for future use.	85	161	1	TO	2 or 3	CardBus spec.
A17/ CAD16	PCMCIA socket address 17 output. In CardBus mode, this pin is the CardBus address/data bit 16.	83	158	1	I/O	2 or 3	CardBus spec.
A16/ CCLK#	PCMCIA socket address 16 output. In CardBus mode, this pin supplies the clock to the inserted card.	93	169	1	I/O	2 or 3	CardBus spec.
A15/ CIRDY#	PCMCIA socket address 15 output. In CardBus mode, this pin is the CardBus IRDY# signal.	95	171	1	I/O-PU	2 or 3	CardBus spec.
A14/ CPERR#	PCMCIA socket address 14 output. In CardBus mode, this pin is the CardBus PERR# signal.	86	162	1	I/O-PU	2 or 3	CardBus spec.
A13/ CPAR	PCMCIA socket address 13 output. In CardBus mode, this pin is the CardBus PAR signal.	84	159	1	I/O	2 or 3	CardBus spec.
A12/ CCBE2#	PCMCIA socket address 12 output. In CardBus mode, this pin is the CardBus C/BE2# signal.	97	173	1	I/O	2 or 3	CardBus spec.
A[11:9]/ CAD[12, 9, 14]	PCMCIA socket address 11:9 output. In CardBus mode, these pin are the CardBus address/data bits 12, 9 and 14, respectively.	77, 73, 80	153, 149, 155	3	I/O	2 or 3	CardBus spec.
A8/ CCBE1#	PCMCIA socket address 8 output. In CardBus mode, this pin is the CardBus C/BE1# signal.	82	157	1	I/O	2 or 3	CardBus spec.
A[7:0]/ CAD[18, 20-26]]	PCMCIA socket address 7:0 outputs. In CardBus mode, these pins are the CardBus address/data bits 18 and 20-26, respectively	100, 103, 105, 107, 109, 111, 113, 116	175, 178, 181, 183, 185, 187, 189, 191	8	I/O	2 or 3	CardBus spec.
D15/ CAD8	PCMCIA socket data/0 bit 15. In CardBus mode, this pin is the CardBus address/data bit 8.	71	148	1	I/O	2 or 3	CardBus spec.
D14 RFU	PCMCIA socket data I/0 bit 14. In CardBus mode, this pin is reserved for future use.	69	145	1	I/O	2 or 3	2 mA

D[13:3]/ CAD[6, 4, 2, 31, 30, 28, 7, 5, 3, 1, 0]	PCMCIA socket data I/0 bits 13:3. In CardBus mode, this pin is the CardBus address/data bit 6 4, 2, 31, 30, 28, 7, 5, 3, 1, and 0, respectively.	67, 65, 63, 124, 122, 120, 68, 66, 64, 62, 59	142, 140, 138, 199, 197, 195, 144, 141, 139, 137, 135	11	I/O	2 or 3	CardBus spec.
D2/ RFU	PCMCIA socket data I/O bit 2. In CardBus mode, this pin is reserved for future use.	123	198	1	I/O	2 or 3	CardBus spec.
D[1:0]/ CAD[29,27]	PCMCIA socket data I/O bits 1:0. In CardBus mode, these pins are the CardBus address/data bits 29 and 27, respectively.	121, 119	196, 194	2	I/O	2 or 3	CardBus spec.
-OE/ CAD11	**Output Enable**: This output goes active (low) to indicate a memory read from the PCMCIA socket to the OZ6833. In CardBus mode, this pin is the CardBus address/data bit 11.	75	151	1	I/O	2 or 3	CardBus spec.
-WE/ CGNT#	**Write Enable**: This output goes active (low) to indicate a memory write from the OZ6833 to the PCMCIA socket. In CardBus mode, this pin is the CardBus GNT# signal.	89	165	1	TO	2 or 3	CardBus spec.
-IORD/ CAD13	**I/O Read**: This output goes active (low) for I/O reads from the socket to the OZ6833. In CardBus mode, this pin is the CardBus address/data bit 13.	78	154	1	I/O	2 or 3	CardBus spec.
-IOWR/ CAD15	**I/O Write**: This output goes active (low) for I/O writes from the OZ6833 to the socket. In CardBus mode, this pin is the CardBus address/data bit 15.	81	156	1	I/O	2 or 3	CardBus spec.
WP/ -IOIS16/ CCLKRUN#	**Write Protect / I/O Is 16-Bit**: In Memory Card Interface mode, this inputs is interpreted as the status of the write protect switch on the PCMCIA card. In I/O Card Interface mode, this input indicates the size of the I/O data at the current address on the PCMCIA card. In CardBus mode, this pin is the CardBus CLKRUN# signal, which starts and stops the CardBus clock CCLK. To enable the CLKRUN# signal, you need to enable ExCA register 3B bit[3:2].	125	201	1	I/O-PU	2 or 3	CardBus spec.
-INPACK/ CREQ#	**Input Acknowledge**: The -INPACK function is not applicable in PCI bus environments. However, for compatibility with other Cirrus Logic products, this pin should be connected to the PCMCIA socket's -INPACK pin. In CardBus mode, this pin is the CardBus REQ# signal.	110	186	1	I-PU	2 or 3	CardBus spec.
RDY/ -IREQ/ CINT#	**Ready / Interrupt Request**: In Memory Card Interface mode, this input indicates to the OZ6833 that the card is either ready or busy. In I/O Card Interface mode, this input indicates a card interrupt request. In CardBus mode, this pin is the CardBus Interrupt Request signal. This signal is active-low and level-sensitive.	91	167	1	I-PU	2 or 3	CardBus spec.
-WAIT/ CSERR#	**Wait**: This input indicates a request by the card to the OZ6833 to halt the cycle in progress until this signal is deactivated. In CardBus mode, this pin is the CardBus SERR# signal.	108	184	1	I-PU	2 or 3	CardBus spec.
CD[2:1]/ CCD[2:1]#	**Card Detect**: These inputs indicate to the OZ6833 that a card is in the socket. They are internally pulled high to the voltage of the +5V power pin. In CardBus mode, these inputs are used in conjunction with CVS[2:1] to detect the presence and type of card.	126, 61	202, 136	2	I-PU-Schmitt	1	CardBus spec.
-CE2/ CAD10	**Card Enable** pin is driven low by the OZ6833 during card access cycles to control byte/word card access. -CE1 enables even-numbered address bytes, and -CE2 enables odd-numbered address bytes. When configured for 8-bit cards, only -CE1 is active and A0 is used to indicate access of odd- or even-numbered bytes. In CardBus mode, this pin is the CardBus address/data bit 10.	74	150	1	I/O	2 or 3	CardBus spec.

Pin Name	Description						
-CE1/ CCBE0#	**Card Enable** pin is driven low by the OZ6833 during card access cycles to control byte/word card access. -CE1 enables even-numbered address bytes, and -CE2 enables odd-numbered address bytes. When configured for 8-bit cards, only -CE1 is active and A0 is used to indicate access of odd- or even-numbered bytes. In CardBus mode, this pin is the CardBus C/BEO# signal.	70	147	1	I/O	2 or 3	CardBus spec.
RESET/ CRST#	**Card Reset**: This output is low for normal operation and goes high to reset the card. To prevent reset glitches to a card, this signal is high-impedance unless a card is seated in the socket, card power is applied, and the card's interface signals are enabled. In CardBus mode, this pin is the RST# input to the card, which is active-low.	106	182	1	TO	2 or 3	CardBus spec.
BVD2/ -SPKR/ -LED/ CAUDIO	**Battery Voltage Detect 2 / Speaker / LED**: In Memory Card Interface mode, this input serves as the BVD2 (battery warning status) input. In I/O Card Interface mode, this input can be configured as a card's -SPKR binary audio input. For ATA or non-ATA (SFF-68) disk-drive support, this input can also be configured as a drive-status LED input. In CardBus mode, this pin is the AUDIO input from the card.	114	190	1	I-PU	2 or 3	-
BVD1/ -STSCHG/ -RI/ -CSTSCHG	**Battery Voltage Detect 1 / Status Change / Ring Indicate**: In Memory Card Interface mode, this input serves as the BVD1 (battery-dead status) input. In I/O Card Interface mode, this input is the -STSCHG input, which indicates to the OZ6833 that the card's internal status has changed. If bit 7 of the **Interrupt and General Control** register is set to `1`, this pin serves as the ring indicate input for wakeup-on-ring system power management support. In CardBus mode, this pin is the CardBus Status Change used by the card to alert the system to changes in READY, WP, and BVD [2:1].	118	192	1	I-PU	2 or 3	-
VS2/ CVS2	**Voltage Sense 2:** This pin is used in conjunction with VS1 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the +5V power pin under the combined control of the external data write bits and the CD pull up control bits. This pin connects to PCMCIA socket pin 57.	104	179	1	I/O-PU	1	CB-spec
VS1/ CVS1	**Voltage Sense 1:** This pin is used in conjunction with VS2 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the +5V power pin under the combined control of the external data write bits and the CD pull up control bits. This pin connects to PCMCIA socket pin 43.	76	152	1	I/O-PU	1	CB-spec
SOCKET_VCC	Connect these pins to the Vcc supply of the socket (pins 17 and 51 of the respective PCMCIA socket). These pins can be 0, 3.3, or 5 V, depending on card presence, card type, and system configuration. The socket interface outputs (listed in this table, Table 2-2) will operate at the voltage applied to these pins, independent of the voltage applied to other OZ6833 pin groups.	117, 98, 60	200, 160, 143	3	PWR	-	-

[1]To differentiate the sockets in the pin diagram, all socket- specific pins have either A_ or B_ prepended to the pin names indicated.
For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.
[2]When a socket is configured as an ATA drive interface, socket interface pin functions change.

Power Control and General Interface Pins

Name	Pin No.	Type	Input	Power Rail	Drive (mA)	Definition
SPKR_OUT	128	I/O	TTL	1	12mA	**Speaker Output**
	Speaker Output: This output can be used as a digital output to a speaker to allow a system to support PC Card fax/modem/voice and audio sound output. This output is enabled by setting the socket's **Misc Control 1** register bit 4 to "1" (for the socket whose speaker signal is to be directed from BVD2/-SPKR/-Led to this pin). This pin is used for configuration information during hardware reset.					
LED_OUT /SKTA_ACTV	133	I/O	TTL	1	12 mA	**LED Output/SKT_ACTV**
	LED Output/SKTA_ACTV: This output can be used as an LED driver to indicate disk activity when a socket's BVD2/-SPKR/-LED pin has been programmed for LED support. In the O2 Mode(Index 3B/7B bit 5) , this pin indicates the socket A activity.The socket B activity refers to PCI Configuration Register offset 90h (Mux Control register)					
CPWRCLK /A_VCC5#	132	I/O	TTL	1	12mA	**Serial Clock / A_VCC5#**
	Card Power Clock: This input is used as a reference clock (10-100 kHz, usually 32 kHz) to control the serial interface of the socket power control chips. A_VCC5# :This active-LOW output controls the 5 -volt supply to the A socket's VCC pins. The active-LOW level of this output is mutually exclusive with that of -VCC_3.					
CPWRDATA/ SMBDATA /B_VCC3#	131	I/O	TTL	1	12mA	**Serial Data / System Management Bus Data/B_VCC3#**
	Card Power Serial Data / System Management Bus Data : This pin serves as output DATA pin when used with the serial interface of Texas Instruments' TPS2202IDF socket power control chip and serves as a bi-directional pin SMBDATA when used with Intel's System Management Bus used by Maxim's socket power control chip. B_VCC3# :This active-LOW output controls the 3.3-volt supply to the A socket's VCC pins. The active-LOW level of this output is mutually exclusive with that of -VCC_5.					
CPWRLATC / SMBCLK /B_VCC5#	130	I/O	N/A	1	12mA	**Serial Latch / System Management Bus Clock /B_VCC5#**
	Card Power Serial Latch / System Management Bus Clock : This pin serves as output LATCH pin when used with the serial interface of Texas Instruments' TPS2202IDF socket power control chip and serves as a bi-directional pin SMBCLK when used with Intel's System Management Bus used by Maxim's socket power control chip. B_VCC5# :This active-LOW output controls the 5 -volt supply to the A socket's VCC pins. The active-LOW level of this output is mutually exclusive with that of -VCC_3.					
A_VCC3#	87	TO	N/A	1	4mA	**A_VCC3#**
	This active-LOW output controls of the 3.3-volt supply to the socket's VCC pins. The active-LOW level of this output is mutually exclusive with of VCC_5#. **This mode active only in SktPwr Parallel mode enabled**					
A_VPP_VCC	115	TO	N/A	1	4mA	**VPP_VCC**
	VPP_VCC: This active-HIGH output controls the socket A VCC supply to the socket's VPP1 and VPP2 pins. The active-HIGH level of this output is mutually exclusive with that of VPP_PGM. **This mode active only in SktPwr Parallel mode enabled**					
B_VPP_VCC	146	TO	N/A	1	4mA	**VPP_VCC**
	VPP_VCC: This active-HIGH output controls the socket B VCC supply to the socket's VPP1 and VPP2 pins. The active-HIGH level of this output is mutually exclusive with that of VPP_PGM. **This mode active only in SktPwr Parallel mode enabled**					

Power, Ground, and Reserved Pins

Name	Pin No.	Type	Input	Power Rail	Drive (mA)	Definition
Aux_Vcc	127	PWR	N/A	-	-	**Auxiliary VCC**
	This pin is connected to the system's 5-volt power supply. In systems where 5 volts is not available, this pin can be connected to the system's 3.3-volt supply if your PCI_VCC and CORE_VCC connected to 3.3V					
CORE_Vcc	134, 79,180	PWR	N/A	-	-	**CORE_VCC**
	This pin provides power to the core circuitry of the OZ6833. It could be connected to a 3.3 power supply.					
CORE_GND	26, 14, 28, 44, 57, 101, 129, 177	GND	N/A	-	-	**CORE_GND**
	All OZ6833 ground pins should be connected to system ground.					

Legend

I/O Type	Description	Power Rail	Source of Output's Power
I	Input Pin	1	AUX_VCC: outputs powered from AUX_VCC
I-PU	Input pin with internal pull-up	2	A_SLOT_VCC: outputs powered from the socket A
O	Output	3	B_SLOT_VCC: outputs powered from the socket B
OD	Open-drain	4	PCI_VCC: outputs powered from PCI bus power supply
TO	Tri-state output	5	CORE_VCC: outputs powered from the CORE_VCC
TO-PU	Tri-state output with internal pull-up		
OD-PU	Open-drain output with internal pull-up		
PW	Power pin		

INTRODUCTION TO OZ6833

Architectural Overview

This section gives a general overview of the architecture of O$_2$Micro's OZ6833. It describes the OZ6833's interface with PCI and PCMCIA sockets, windowing, built-in power management features, interrupts, and Interface I/O Register Addressing.The OZ6833 is a Yenta, PCI-2.1, PCMCIA 2.1, JEIDA-4.2, and ExCA compliant PCMCIA controller. O$_2$Micro's OZ6833 is the solution for today's notebook PCs. It requires no external buffers and can be directly connected to the PC card sockets, thus ensuring the minimal real estate requirement of today's notebook or handheld market. The OZ6833 allows OEMs to design their systems to provide the PC user with a wide range of connectivity options (Modem, Twisted Pair Ethernet, Floppy disk, etc.) as well as eliminating rotating electro-mechanical media (via the widely abundant Flash Memory Cards on the market).

The OZ6833 maintains the 16-bit PC Card physical designs and provides backward compatibility with 16-bit PC cards. The OZ6833 detects when a 16-bit PC Card is inserted into a card socket and configures the socket to provide compatibility with the 16-bit PC Card. When a CardBus card is inserted into the card socket, the system configures the interface to provide the same enhanced capabilities available to 32-bit PCI devices (including bus mastering). The OZ6833 provides a point-to-point connection between the card socket and CardBus bridge which permits a maximum theoretical throughput of 132MB/second.

The OZ6833 allows memory and I/O devices to be inserted any time as exchangeable peripherals into the PC sockets. OZ6833 provides 5 programmable memory windows and 2 programmable I/O windows to map the inserted PC cards into the system memory and I/O space. PC cards have both attribute and common memory. Attribute memory is used to indicate to host software the capabilities of the PC Card and to allow host software to change the configuration of the PC Card. Common memory can be used for any purpose that the host software can interpret (flash file system, system memory, floppy emulation, etc.). I/O PC Cards, such as Modem and Ethernet Cards, are supported as if they were I/O devices on the system motherboard. I/O devices, which usually requires generation of interrupts are not limited by interrupt lines that are available. Each interrupt generated by the PC Cards can be steered to several of the standard IRQ lines generated by the OZ6833.

PCI Interface

The OZ6833 is a PCI-To-CardBus bridge chip. The OZ6833 functions as a PCI slave device transferring I/O and memory cycles on PCI to PCMCIA for 16-bit PC Card Interface and for 32-bit CardBus card OZ6833 function as a PCI-TO-PCI bridge. The OZ6833 does a positive decode of the address provided by the memory and I/O window registers. The CardBus Socket registers and PCMCIA ExCA I/O internal registers are accessed by programming the PC Card Socket Status and Control Registers Base Address Register 0 and the 16-bit PC Card legacy Mode Base Address Register.

PCMCIA Socket Interface

The PCMCIA/JEIDA interface consists of 60 signals and 8 power connections that interface to PC cards

through a 68 pin socket. Each OZ6833 can be configured to support up to two PC cards sockets directly, with the provision to allow up to eight PC card sockets in multiples of two. The OZ6833 supports two PC card types (either memory or I/O) interchangeably. It accomplishes this by multiplexing some of the static signals that are defined differently for memory and I/O PC cards. These signal are configured appropriately by accessing the PC card's configuration registers.

Memory and I/O Window Mapping

Memory address mappings for the OZ6833 bridge are on 4Kbyte boundaries with a minimum mapping of 4 Kbytes. The OZ6833 may be mapped anywhere within the address space assigned to the bridge. The OZ6833 provides two memory base and limit register pairs which may be used for mapping memory mapped I/O or prefetchable memory space. Two I/O mapping register pairs are provided for each socket, allowing some fragmenting of I/O space on a card and interleaving of I/O space with other I/O devices. Multiple PC cards in a system can conflict if they try to utilize the same system memory and I/O range. The OZ6833 allows mapping of each PC card into a separate memory range, and a separate I/O range either through the use of the 5 programmable memory windows and the 2 programmable I/O windows for 16-bit PC cards or through two memory or I/O windows for 32-bit CardBus cards thus avoiding system configuration
conflicts. The OZ6833 provides memory paging, memory address mapping for both PC card attribute and common memory, and I/O address mapping. The OZ6833 includes registers to allow access to the card information structure and card configuration registers within the attribute memory described by the PCMCIA/JEIDA PC card Standard.

Power Management

The OZ6833 implements power management for each PC card socket. Socket power management is controlled through programming the POWER and RESETDRV control register.

The OZ6833 will automatically enter into lower power consumption state when memory windows

and I/O windows are disabled, and when sockets become empty.

A unique feature is provided by the OZ6833 to support the host system suspend/resume operation. During suspend mode, if an previously inserted 5V card is swapped with a lower voltage card, an improper voltage will then be applied to the new, lower voltage card thus damaging the PC card. The OZ6833 provides a mechanism internal to the chip to automatically resense the proper voltage that needs to be applied to the PC card once the system is resumed. This mechanism protects the PC cards from any accidental removal and insertion of the card during suspend mode when the controller is normally unaware of such change.

ACPI – PCI BUS Power Management Interface

The OZ6833 is compliant with the ACPI-PCI Bus Power Management Interface Specification for PCI to CardBus Bridges and Device Class Power Management Reference Specification –PC Card Controller Device Class. The OZ6833 supports the D0, D1, D2 and D3 states and PME# pin. The whole Power Management Register Block is located at PCI configuration register A0h and A4h . The ACPI O/S can program the OZ6833 into the different power saving states (D1 or D2 or D3) based on the whole system activity on the PCMCIA/CardBus interface. Any Wake Event will request the O/S to bring back to the full on state D0 through the PME#. Systems must route the PME# signal to the appropriate system logic to wake the system. For example, an ACPI compliant systems may route this signal to the SCI# interrupt. Please refer our PME# application note for detail.

Socket Power Control

The OZ6833 supports two types of Socket Power Control modes.

- Parallel Socket Power Control Mode.
- Serial Socket Power Control Mode.

Parallel Socket Power Control Mode :

The OZ6833 supports conventional parallel interface to socket power control devices. The

OZ6833 generates the four pins VPP_VCC, VPP_PGM, VCC_3#, VCC_5# for each socket to control the socket power.

Serial Socket Power Control Mode:

The OZ6833 provides two pins to serially control the socket power. Following are the three socket power control modes supported by the OZ6833.

- Texas Instruments TP2202IDF Serial Signaling Mode
- System Management Bus Signaling Mode

The socket power-control signaling mode is usually established during power-on reset the level on SDATA/SMBDATA and SLATCH/SMBCLK.

Texas Instruments TP2202IDF Serial Signaling Mode:

In this mode, the OZ6833 supports the Texas Instruments TP2202IDF dual-socket PC Card power interface switch. The OZ6833 uses three-pins for this mode. The pin SCLK is usually connected to 32-kHz clock which is available on the system. The SCLK serves as a reference clock for the OZ6833 and as a clock to the TP2202IDF. The data is serially transferred over SDATA and the latch signal is SLATCH.

System Management Bus Signaling Mode:

In this mode, the OZ6833 supports the Intel System management BUS (SMB) protocol. The serial data is available on the SMBDATA pin and the serial clock is on the SMBCLK pin. The SCLK pin is used as a reference clock for the OZ6833. The Maxim MAX 1601 dual-channel PC Card network supports the SMB protocol.

Interrupt Support

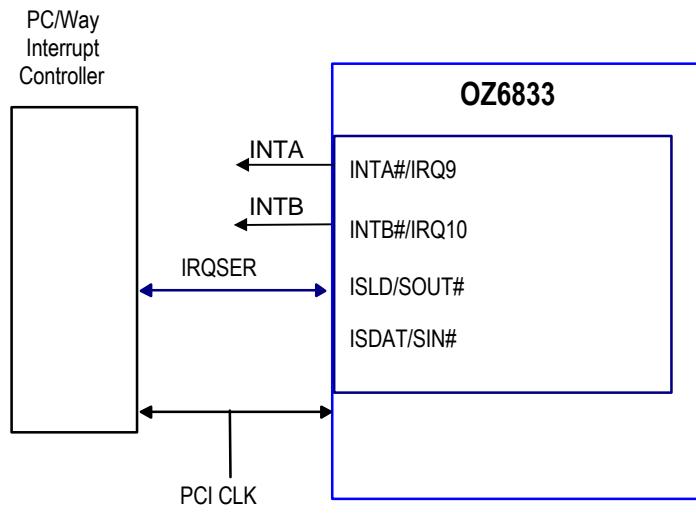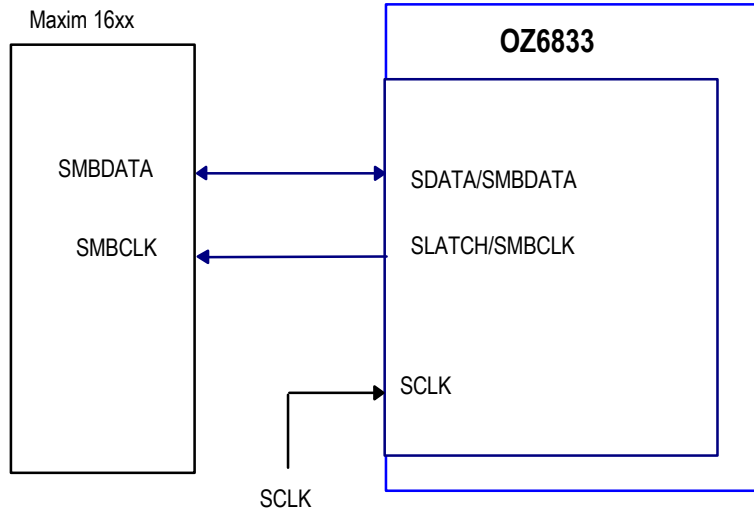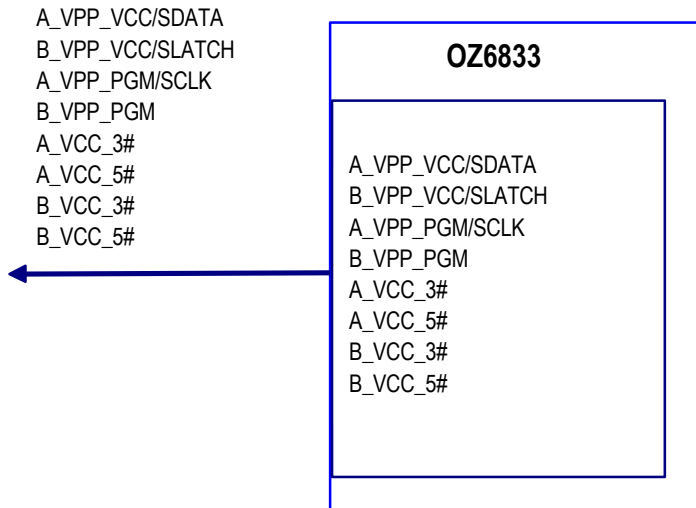The OZ6833 has four different ways to generate the interrupts to the interrupt controller.

- PCI Interrupt Mode
- PC/PCI Interrupt Mode
- PCI/Way Interrupt Mode
- VESA Serialized IRQ

PCI Interrupt Mode:

In this mode, the internal IRQ interrupts are routed to the PCI INTA# and INTB#. The ten interrupts can be routed and be shared to PCI INTA# and INTB# signals for socketA and socketB card status change interrupts and Card function interrupts.

PC/PCI Interrupt Mode:

This mode supports the mobile PC/PCI Extended Programming Mode. In this mode two pins are provided for SIN# and SOUT# which interface with SIC(serial interrupt controller to support all ISA IRQs . The SIC is clocked by PCI clock.

PCI/Way Interrupt Mode:

In this mode the OZ6833 provides a IRQ serializer pin to the interrupt controller. The IRQSER is simply a wired-or structure that replicates the state of each internal IRQ. This signal is bi-directional. With PCI INTA# & INTB# pins and IRQSER , the OZ6833 can support all ISA IRQs and PCI interrupts to meet Microsoft PC97 requirement.

VESA Serialized IRQ :

This is similar to PCI/WAY Interrupt mode. It uses only one IRQSER pin to cover all ISA interrupt IRQ0-IRQ15 and PCI INTA#, INTB#, INTC# and INTD#. You can enable this mode by PCI Configuration register 90h bit[16] and bit[12:10]

WIN'97 IRQ Support

In compliance to the latest PC 97 guidelines, O2Micro's OZ6833 supports simultaneous configuration of both ISA and PCI Interrupt modes for maximum design flexibility. With WIN97 IRQ Support bit (bit 10 of CardBus Socket Status & Control Register - Offset:28H), the OZ6833 CardBus Bridge is configurable to utilize ISA Interrupt mode for PC Card 16 cards and PCI Interrupt mode for PC Card 32 cards concurrently.

When WIN97 IRQ Support bit is set, R2 Card (PC Card 16 card) is in either PC/PCI or PCI/Way Interrupt modes selectable through the System Interrupt Mode bits (bit [1:0] of O2Micro Mode Control D Register), while R3 Card (PC Card 32 card) is always in PCI Interrupt mode. For R2 Card with PC/PCI Interrupt mode, INTC# and INTD# are dedicated as SOUT# and SIN#, respectively. If R2 Card is configured for PCI/Way Interrupt mode, INTC# is used as IRQSER interrupt while INTD# is not used. For R3 Card in PCI Interrupt mode, INTA# and INTB# are used as interrupts for Socket A and Socket B, respectively.

Interface I/O Register Addressing

All the OZ6833 Socket Status & Control Registers for 32 Bit PC Cards can be accessed through PC Card Socket Status and Control Registers Base Address.
(Configuration Register 10h) offset 00h to 7FFh. The ExCA registers implemented in the OZ6833 can
be accessed via PC Card Socket Status and Control Registers Base Address (Configuration Register 10h) offset 800h to FFFh or via the 16-bit PC Card Legacy Mode Base Address Register (Configuration Register 44h) for 16-bit PC Cards.

For via the 16-bit PC Card Legacy Mode Base Address Register ,the first I/O address (16-bit PC Card Legacy Mode Base Address Register) is the OZ6833's index register. The second I/O address (16-bit PC Card Legacy Mode Base Address Register + 01) is the OZ6833's data register.

The index register and the data register are read/write registers. The OZ6833 will not respond to a data register read or write operation or to an index register read operation unless the index register has first been written to with a valid index.
Refer to PCI Memory Address Space Table.

Programmable Output pin for Ring-out, SocketA-Activity & SocketB-Activity

The OZ6833 can provide the programmable pin location mux with IRQs for Ring-out, SocketA-Activity and SocketB-Activity.

The Ring-out pin pulse mode directly reflects PCMCIA/CardBus Ring-in pin. This Ring-out pin is for system wake-up during suspend mode. The ACPI/PC97 requires this Ring-out function and feature.

SocketA-Activity and SocketB-Activity can be directly connected to system core logic chipset as external peripheral activity for suspend/ resume or you can use these two outputs to drive the LCD Icon Display driver for PCMCIA/ CardBus activity.
Refer to PCI Configuration Register 90h (Mux Control Register)

PCI 2.1 Subsystem Vendor ID to meet PC 98 requirements

The OZ6833 meets the PC 98 requirements for Subsystem Vendor ID support. There are two methods to implement a subsystem vendor ID : a device vendor can either use serial ROMs to fill the value into the registers, or program the Subsystem Vendor ID using BIOS. Two designs using the BIOS method meet PC 98 requirements :

- Make a copy of the Subsystem Vendor ID in PCI user-defined space. Any writes to this location will change both the copy and the Subsystem Vendor ID field. Any writes to the Subsystem Vendor ID are discarded.

- Make a write-enable bit in the PCI user-defined space. The BIOS can turn this bit on, change the Subsystem Vendor ID, then turn it off.
Refer to the Subsystem Vendor ID application note for detail.

Interrupt Modes for OZ6833:

PCI

| OZ6833 |

INTA# INTA#/IRQ9

INTB# INTB#/IRQ10

ISLD

ISDAT

PCI Interrupt Mode

PC/PCI SIC
Controller

| OZ6833 |

INTA INTA#/IRQ9

INTB INTB#/IRQ10

SOUT# ISLD/SOUT#

SIN# ISDAT/SIN#

PCI CLK

PC /PCI Interrupt Mode

PC/Way
Interrupt
Controller

OZ6833

INTA   INTA#/IRQ9

INTB   INTB#/IRQ10

IRQSER   ISLD/SOUT#

ISDAT/SIN#

PCI CLK
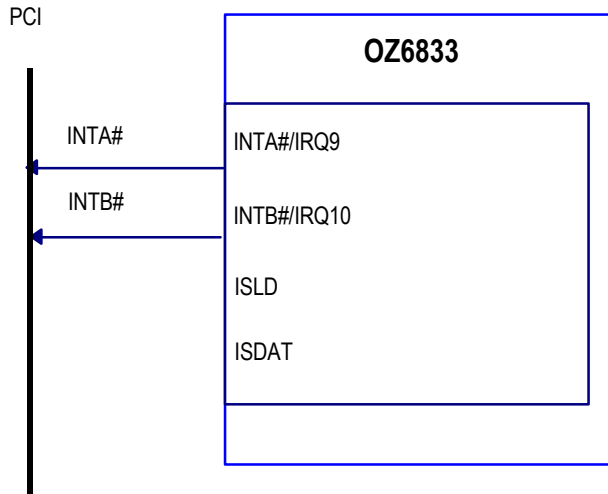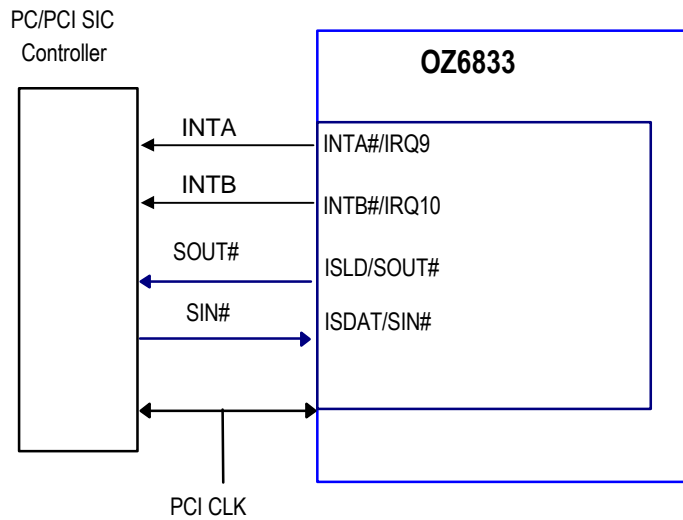
PCI/Way Interrupt Mode

Socket Power Control Modes for OZ6833:

TI2202

OZ6833

SDATA ← SDATA/SMBDATA

SLATCH ← SLATCH/SMBCLK

SCLK ←→ SCLK

SCLK
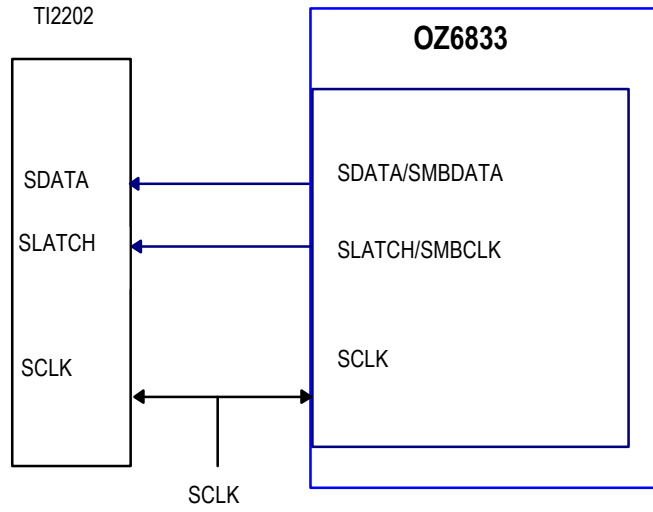
Texas Instruments TPS2202IDF Serial Signaling Mode

Maxim 16xx

OZ6833

SMBDATA   →   SDATA/SMBDATA

SMBCLK   ←   SLATCH/SMBCLK

SCLK → SCLK

SCLK

System Management Bus Signaling Mode

A_VPP_VCC/SDATA
B_VPP_VCC/SLATCH
A_VPP_PGM/SCLK
B_VPP_PGM
A_VCC_3#
A_VCC_5#
B_VCC_3#
B_VCC_5#

OZ6833

A_VPP_VCC/SDATA
B_VPP_VCC/SLATCH
A_VPP_PGM/SCLK
B_VPP_PGM
A_VCC_3#
A_VCC_5#
B_VCC_3#
B_VCC_5#

PCMCIA Power Control Parallel Mode

PCI CONFIGURATION REGISTERS

The OZ6833 has two separate configurated spaces. There is one implemented for each socket. The second socket is the second function and starts at 100h. When configured as a two slot CardBus bridge, the bridge has two configuration spaces, Function 0 is for Socket A(0), Function 1 is the CardBus configuration for Socket B(1). The OZ6833 has been defined as closely as possible to PCI-to PCI Bridge. PCMCIA ExCA registers are accessed though either Memory Base Address Register or the Legacy Mode Base Address Register.

CAUTION: If bits indicated as read only (R:) are to be written to, they should be written to zero.

CardBus Bridge Configuration Registers

Byte

3	2	1	0	
Device ID		Vendor ID		00
Status Register		Command Register		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
PC Card Socket Status/Control Registers Base Address				10h
Secondary Status		Reserved		14h
CardBus Latency Timer	Subordinate Bus Number	CardBus Bus Number	PCI Bus Number	18h
Memory Base Register 0				1Ch
Memory Limit Register 0				20h
Memory Base Register 1				24h
Memory Limit Register 1				28h
I/O Base Register 0 Upper Half		I/O Base Register 0 Lower Half		2Ch
I/O Limit Register 0 Upper Half		I/O Limit Register 0 Lower Half		30h
I/O Base Register 1 Upper Half		I/O Base Register 1 Lower Half		34h
I/O Limit Register 1 Upper Half		I/O Limit Register 1 Lower Half		38h
Bridge Control		Interrupt Pin	Interrupt Line	3Ch
Subsystem ID		Subsystem Vendor ID		40h
PC Card 16-Bit IF Legacy Mode Base Address				44h

Vendor ID and Device ID (Offset :00h, 100h)

BIT POSITION	NAME	DESCRIPTION
15-0	Vendor ID	This read-only field is the Vendor identification assigned to O$_2$Micro by the PCI Special Interest Group. This field will always read back 1217h.
31-16	Device ID	This read-only field is the device identification assigned to this device by O$_2$Micro. This field will always read back 6832 for the OZ6833. (Revision number identification for the OZ6833 part itself is indicated by the Revision ID field in the **Revision ID** and **Class Code** register at offset 08h.

Command and Status(Offset : 04h, 104h)

BIT POSITION	NAME		DESCRIPTION
0	8	0	The I/O space for the OZ6833 is disabled. Any reads or writes to the I/O space will be ignored. This applies to both the I/O registers of the OZ6833 itself as well as any I/O windows that might have been enabled to the PCMCIA sockets.
			The I/O specs for the OZ6833 is enabled and will respond to reads and writes to the I/O address range defined in Base Address 0 register as well as any I/O window addresses.
1	PCI Memory Space Enable	0	The memory space for the OZ6833 is disabled. Any reads or writes to the memory space will be ignored. This applies to both the memory registers of the OZ6833 itself, as well as any memory windows which might have been enabled to the PCMCIA sockets.
		1	The memory space for the OZ6833 is enabled, allowing memory window access.
4	Capabilities List	1	This bit indicates a list of new PCI Power Management Capabilities is implemented. Register at 14h provides an offset into the PCI Configuration Space pointing to the location of the first item in the Capabilities list.
6	Parity Error Check/Report Enable	0	Disables parity checking reporting in the OZ6833.
		1	Enables parity checking reporting in the OZ6833.
7	Wait Cycle Enable		This bit will always read "1", indicating that the OZ6833 employs address stepping.
8	System Error (SERR#) Enable		This bit enables the OZ6833's reporting of system errors by assertion of the SERR# pin when address parity errors occur. Bit 6 must also be set to "1" to allow detecting of conditions that allow SERR# activation. See also description of bit 30.
		0	Disables activation of SERR# on address parity error.
		1	Enables SERR# activation whenever an address parity error is internally detected (slave mode).
16-19	Read Only	0h	Reserved
20	Read Only	1 (default)	Capabilities List - This bit indicates whether this function implements a list of extended capabilities such as PCI Power Management. When set this bit indicates the presence of a Capabilities List. OZ6833 supports the Capabilities List.
21-23	Reserved	0h	This bit is Reserved and will always read "0".
24	Master Data Parity Error Reported		This bit is Reserved and will always read "0".
26-25	DEVSEL# Timing		The OZ6833 always responds as a medium-speed device. Thus, this field always reads back "01".
30	System Error (SERR#) Generated		This bit is set whenever the OZ6833 asserts SERR# because of internal detection of a PCI address parity error. Bit 8 of this register must be set before system errors can be reported, and bit 6 must be set to allow address parity errors to be detected. The OZ6833 only asserts SERR# if address parity errors occur. No other chip or system action will cause SERR# to be driven active.
		0	SERR# not asserted by this device.
		1	SERR# was asserted by this device, indicating a PCI address parity error.
31	Address/Data Parity Error Detected		This bit indicates whether a parity error was detected, independent of whether the OZ6833 is in bus master mode or whether bit 6 of this register is a "1".
		0	No data parity errors detected.
		1	Address or data parity error detected.

Revision ID and Class Code (Offset : 08h, 108h)

BIT	NAME	DESCRIPTION

©OZ6833-DS-1.2

POSITION		
7-0	Revision ID	This read-only field identifies the revision level of the OZ6833 chip. It will read back 3xh
31-8	Class Code	This read-only field identifies the OZ6833 as a PCI-to PCMCIA bridge device. It will read back 060700h.

Cache Line Size, Latency Timer, Header Type, and BIST (Offset : 0Ah, 10Ah)

BIT POSITION	NAME	DESCRIPTION
23-16	Header Type	This read-only field specifies that OZ6833 is a multi-function PCI to CardBus device. It will always read back 82h.

Base Address 0 (Offset : 10h, 110h)

BIT POSITION	NAME	DESCRIPTION
31-0	Base Address	This register points to the memory mapped I/O space that contains both the CardBus and 16-bit Status and Control registers. CardBus Status and Control registers start at offset 000h and the 16-bit card registers start at offset 800h. Bits [31:11] are R/W. Bits [11:00] are hardwired to zero. This indicates to configuring software that the bridge wants 4K bytes of non-prefetchable memory space, starting on a 4K boundary, that can be mapped anywhere in memory. This register's bits adhere to the definitions set out in the PCI Local Bus Specification.

Capabilities Pointer, Cap_Ptr (Offset : 14, 114h)

BIT POSITION	NAME	DESCRIPTION
7-0	Cap_Ptr	Default Read Only value is A0h. This register provides an offset into the PCI's Configuration Space for the location of the first item in the Capabilities Linked List.

(Offset : 15h, 115h)

BIT POSITION	NAME	DESCRIPTION
15-0	Reserved	Read back 0000h

Secondary Status (Offset : 16h, 116h)

BIT POSITION	NAME	DESCRIPTION
31-16	Secondary Status	The Secondary Status Register is similar in function to the Primary Status Register but contains information relating to the CardBus. Bit 14 of this register is defined differently than the Primary. When set it indicates that the bridge has detected SERR# asserted on the CardBus. This function is identical to that specified in the PCI to PCI bridge specification.

PCI Bus Number (Offset : 18h, 118h)

BIT POSITION	NAME	DESCRIPTION
7-0	PCI Bus Number	The Primary Bus Number identifies the number of the PCI Bus on the Primary side of the bridge. This is set by the appropriate configuration software.

CardBus Bus Number (Offset : 19h, 119h)

BIT	NAME	DESCRIPTION

BIT POSITION		
15-8	CardBus Bus Number	The CardBus Bus Number identifies the number of the CardBus attached to the socket. This is set by PCI BIOS configuration software or Socket Services software. This register is called the "secondary Bus Number" on a PCI to PCI bridge.

Subordinate Bus Number (Offset : 1Ah, 11Ah)

BIT POSITION	NAME	DESCRIPTION
23-16	Subordinate Bus Number	The Subordinate Bus Number is a register defined for PCI to PCI bridges. It holds the number of the bus at the lowest part of the hierarchy behind the bridge. Normally, a CardBus bridge will be at the bottom of the bus hierarchy and this register will hold the same value as the CardBus Bus Number register.

CardBus Latency Timer (Offset : 1Bh, 11Bh)

BIT POSITION	NAME	DESCRIPTION
31-24	CardBus Latency Timer	The CardBus Latency Timer has the same functionality of the primary PCI Bus Latency Timer but applies to the CardBus attached to this specific socket. This is set by PCI BIOS configuration software or Socket Services Software.

Memory Base #0(Offset : 1Ch, 11Ch)

BIT POSITION	NAME	DESCRIPTION
31-0	Memory Base #0	The Memory Base register defines the bottom address of a memory mapped I/O space. The upper 20 bits of this register correspond to AD[31:12]. The bottom 12 bits of this register are read only and return zero when read. This window is enabled by bit #1 of the Command register. Prefetching within this window is controlled by bit #8 of the Bridge Control register. The default is enabled and should only be cleared if Memory Reads will cause side effects on the installed cards.

Memory Limit #0 (Offset : 20h, 120h)

BIT POSITION	NAME	DESCRIPTION
31-0	Memory Limit #0	The Memory Limit register defines the top address of a memory mapped I/O space. The upper 20 bits of this register correspond to AD[31:12]. The bottom 12 bits of this register are read only and return zeros when read. The bridge assumes the bottom address bits [11:0] are ones to determine the range defined. Both Memory Windows are enabled by Command register bit #1. To disable either windows individually, the Limit register of that range should be set below the Base. This will cause the bridge to never detect a hit on that window.

Memory Base #1(Offset : 24h, 124h)

BIT POSITION	NAME	DESCRIPTION
31-0	Memory Base #1	The Memory Base has the same functionality as Memory Base 0. This window is enabled by bit #1 of the Command register. Prefetching within this window is controlled by bit #9 of the Bridge Control register. The default is enabled and should only be cleared if Memory Reads will cause side effects on the installed card.

Memory Limit #0(Offset : 28h, 128h)

BIT POSITION	NAME	DESCRIPTION
31-0	Memory Limit #0	The Memory Limit 1 register has the same functionality as the Memory Limit 0 register.

I/O Base #0 (Offset : 2Ch, 12Ch)

BIT POSITION	NAME	DESCRIPTION
15-0	I/O Base #0 (Lower 16 Bits)	The I/O Base register defines the bottom address of an address range that is used by the bridge to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[15:0]. Bits AD[1:0] are used to indicate whether the bridge implements 16 or 32 bit I/O addressing. For address decoding, if only 16 bit addressing is implemented the bridge must determine that the upper 16 bits of address are zeros before accepting an access. Address bits AD[15:2] provide the 4 byte granularity required by CardBus. This I/O mapping varies from a PCI to PCI bridge, in that it allows mapping the windows on a 4 byte boundary with a minimum size of 4 bytes. A PCI to PCI bridge maps I/O windows on 4K boundaries with a minimum 4 Kbyte size.

I/O Base #0 (Offset :2Eh, 12Eh)

BIT POSITION	NAME	DESCRIPTION
31-16	I/O Base #0 (Upper 16 Bits)	This optional register is an extension to the I/O Base Register. It defines bits AD[31:16]. The I/O Limit Upper 16 Bits Register are not implemented. I/O devices behind the bridge will all be mapped below 0001 000h and the bridge validates that bits AD[31:16] are all set to zero before accepting an access.

I/O Limit #0 (Offset :30h, 130h)

BIT POSITION	NAME	DESCRIPTION
15-0	I/O Limit #0 (Lower 16 Bits)	The I/O Limit register defines the top address of the address range that is used by the bridge to determine when to forward an I/O access to the CardBus. The bits in this register correspond to AD[15:00].

I/O Limit #0(Offset :32h, 132h)

BIT POSITION	NAME	DESCRIPTION
31-16	I/O Limit #0 (Upper 16 Bits)	This optional register is an extension to the I/O Limit Register.

I/O Base #1 (Offset :34h, 134h)

BIT POSITION	NAME	DESCRIPTION
15-0	I/O Base #1 (Lower 16 Bits)	The I/O Base register defines the bottom address of an address range that is used by the bridge to determine when to forward an I/O transaction to the CardBus. The bits in this register correspond to AD[15:0]. Bits AD[1:0] are used to indicate whether the bridge implements 16 or 32 bit I/O addressing. For address decoding, if only 16 bit addressing is implemented the bridge must determine that the upper 16 bits of address are zeros before accepting an access. Address bits AD[15:2] provide the 4 byte granularity required by CardBus. This I/O mapping varies from a PCI to PCI bridge, in that it allows mapping the windows on a 4 byte boundary with a minimum size of 4 bytes. A PCI to PCI bridge maps I/O windows on 4K boundaries with a minimum 4 Kbyte size.

I/O Base #1(Offset :36h, 136h)

BIT POSITION	NAME	DESCRIPTION
31-16	I/O Base #1 (Upper 16 Bits)	This optional register is an extension to the I/O Base Register. It defines bits AD[31:16]. The I/O Limit Upper 16 Bits Register are not implemented. I/O devices behind the bridge will all be mapped below 0001 000h and the bridge validates that bits AD[31:16] are all set to zero before accepting an access.

I/O Base #1(Offset :38h, 138h)

BIT POSITION	NAME	DESCRIPTION
15-0	I/O Limit #1 (Lower 16 Bits)	The I/O Limit register defines the top address of the address range that is used by the bridge to determine when to forward an I/O access to the CardBus. The bits in this register correspond to AD[15:00].

Interrupt Line, Interrupt Pin, Min_Gnt, and Max_Lat (Offset : 3Ch, 13Ch)

BIT POSITION	NAME	DESCRIPTION
7-0	Interrupt Line	This register is used in the manner defined in the PCI Local Bus Specification and PCI to PCI Bridge Specification.
15-8	Interrupt Pin	Read only register. Bit definition adheres to the PCI Local Bus Specification and PCI to PCI Bridge Specification.
31-24	Reserved	

Bridge Control Register (Offset : 3Eh, 13Eh)

BIT POSITION	NAME	DESCRIPTION
0	Parity Error Response Enable	Controls the response to parity errors on the CardBus. When 0 parity errors are ignored. When set parity on the CardBus is checked and errors reported. Default on reset is zero (disabled).
1	SERR# Enable	Controls forwarding of SERR# signals indicated on the CardBus. When set the bridge will forward to the PCI bus a SERR# indication on the CardBus. Default on reset is zero (disabled).
2	ISA Enable	This applies only to addresses that are enabled by the I/O Base and Limit registers and are also in the first 64 Kbytes of PCI I/O space. When set the bridge will block forwarding from PCI to CardBus I/O transactions addressing the last 768 byte in each 1 Kbyte block. In the opposite direction (CardBus to PCI) I/O transactions will be forwarded if they address the last 768 byte in each 1 K block. Default on reset is zero (disabled).
3	VGA Enable	Modifies the bridge's response to VGA compatible addresses. When the VGA enable bit is set the bridge will forward transactions to the following ranges: Memory: 0A 0000h to 0B FFFFh I/O: Addresses where AD[9:0] are in the ranges 3B0h to 3bbh and 3C0h to 3dFh (inclusive of ISA address aliases; AD[15:10] are not decoded. When the VGA Enable bit is set forwarding of these accesses is independent of both the I/O and memory address ranges. Forwarding is also independent of the setting of the ISA Enable bit in the Control register or the VGA Snoop bit in the Command register. Forwarding of these accesses IS affected by the I/O and Memory Enable bits in the Command register. Default on reset is zero (disabled).
4	Reserved	Returns zero on read.
5	Master Abort Mode	Controls the behavior of the bridge when a master abort occurs on either PCI or CardBus interface when the bridge is master. When not set the bridge must return all ones if a master abort occurs during a read. During a write the data should be dropped in the bit bucket. When the bridge signals a target abort to the requesting master when the corresponding transaction on the opposite bus terminates with a master abort and the transaction on the source side is not complete (reads and non-posted writes). If the transaction on the source bus is complete, and SERR# is enabled in the Command register, the bridge must assert SERR# on the PCI Bus. Default on reset is zero.

6	CardBus Reset	When set the bridge will assert and hold CRST#. When cleared the bridge will deassert CRST#. This bit may be set by software. It will also be set by hardware when the controller executes the powerdown sequence. This bit is cleared only by software. CRST# is a wire-OR of this control bit and PCIRST#.
7	IREQ-INT Enable	When set this bit enables the IRQ routing register for 16 bit cards. When cleared IRQ interrupts will be routed to the INT pin indicated by the Interrupt Pin register. This bit should be cleared by PCIRST#.
8	Memory 0 Prefetch Enable	When set enables Read prefetching from the memory window defined to by the Memory Base 0 and Memory Limit 0 registers. Default on reset is one (enabled).
9	Memory 1 Prefetch Enable	When set enables Read prefetching from the memory window defined to by the Memory Base 1 and Memory Limit 1 registers. Default on reset is one (enabled).
10	Write Posting Enable	Enables posting of Write data to and from the socket. If this bit is not set the bridge must drain any data in its buffers before accepting data for or from the socket. Each data word must then be accepted by the target before the bridge can accept the next from the source master. The bridge must not release the source master, until the last word is accepted by the target. Operating with write posting disabled will inhibit system performance,
11-15	Reserved	Return zero on read.

Subsystem Vendor ID(Offset :40h, 140h)

BIT POSITION	NAME	DESCRIPTION
15-0	Subsystem Vendor	This optional register is identical to that described in Revision 2.1 of the PCI specification. Must return zeros if not implemented. For PC 98 compliance, please see the Subsystem Vendor ID section

Subsystem ID (Offset :42h, 142h)

BIT POSITION	NAME	DESCRIPTION
15-0	Subsystem ID	This optional register is identical to that described in Revision 2.1 of the PCI specification. Must return zeros if not implemented. For PC 98 compliance, please see the Subsystem Vendor ID section

PC Card 16 Bit IF Legacy Mode Base Address(Offset :44h, 144h)

BIT POSITION	NAME	DESCRIPTION
0-31	PC Card 16 Bit IF Legacy Mode Base Address	This optional register points to the index and data registers that resided at 3E1 and 3E0 in the 82365. This register is intended only for legacy mode operation. It is not recommended that this mode be used by new software. New mode should use the PC Card Socket Status and Control registers Base Address space to address the registers directly. This register is cleared and disabled by PCIRST#. It must not respond to the PCI cycles unless specifically loaded with a non-zero address after PCIRST# is deasserted. When this register is enabled memory mapped accesses to the Socket and Control registers, via PC Card Socket Status and Control registers Base Address register, are disabled. This makes useage of this mode and the memory mapped mode mutually exclusive This register's bits adhere to the definitions set out in the PCI Local Bus Specification. Note: The implementation of this optional register does not remove the requirement to support direct memory mapped access to the 16 bit IF Control and Status registers via the PC Card Socket Status and Control registers Base Address at 10h.

Mux Control Register (Offset :90h)

BIT POSITION	NAME	DESCRIPTION
3-0	RING_OUT_MUX	RING_OUT Enable bits : "0000" - Disable "1111" – Enable Ring_Out function also need to set ExCA 03h/43h bit[7] and 16h/56h bit[4] & 39h/79h bit[7]
7-4	SKTB_ACTV_MUX	These bits determine the B_SOCKET_ACTIVITY function To enable the output, bit 9 has to be set to "1". "0000" - Reserved (Default: disabled) "1011" – Enable (to enable the output, bit 9 has to be set to 1).
8	SKTA_ACTV_Enable	"0" = Disable socket A activity LED Output (default) "1" Enable Socket A activity LED Output
9	SKTB_ACTV_Enable	"0" = Disable socket B activity LED Output (default) "1" Enable Socket B activity LED Output
12-10	Serial IRQ (PCI/Way) Hardware interrupt routing table	When Serial IRQ is enabled and PCI interrupts are routed to use serial IRQ outputs, the PCI interrupts can be routed to serial IRQ INTA, INTB, INTB or INTD. These bits determine the routing method: "000" - Socket A interrupt will use Serial IRQ INTA; Socket B interrupt will use Serial IRQ INTB. "001" - Socket A interrupt will use Serial IRQ INTB; Socket B interrupt will use Serial IRQ INTC. "010" - Socket A interrupt will use Serial IRQ INTC; Socket B interrupt will use Serial IRQ INTD. "011" - Socket A interrupt will use Serial IRQ INTD; Socket B interrupt will use Serial IRQ INTA. "100" - Socket A and Socket B will both use Serial IRQ INTA. "101" - Socket A and Socket B will both use Serial IRQ INTB. "110" - Socket A and Socket B will both use Serial IRQ INTC. "111" - Socket A and Socket B will both use Serial IRQ INTD.
13	Reserved	
15-14	Reserved	
16	Include_PCI_IRQ	"0" = (default) PCI interrupts are routed to PCI_INTAN (pin# 248) and PCI_INTBN (pin#249) "1" PCI Interrupts are routed to serial IRQ output. Bit 12 to 10 determine the routing method.
19-18	SKTA_Turbo	"00" – default the PCMCIA command active width 165ns "01" – PCMCIA command active width 80ns "10"-- PCMCIA command active width 40ns "11" - Reserved
21-20	SKTB_Turbo	"00" – default the PCMCIA command active width 165ns "01" – PCMCIA command active width 80ns "10"-- PCMCIA command active width 40ns "11"- Reserved
22	Aux_VCC5N	"0" – default . the Aux_VCC power rail is connected to +5V "1" – The Aux_VCC is connected to 3.3V
23	PCI_VCC3N	"0" – default . the PCI_VCC power rail is connected to +3.3V "1" – The PCI_VCC is connected to 5V
27-24	PME_MUX	These bits determine the PME# function and PCI Configuration register A4h bit[8] "1000" - Reserved (Default: disabled) "1100" – Enable
28	Reserved	
29	Reserved	
31-30	Reserved	

Power Mangement Register (Offset :A0h)

Bits	Default Value	Read/Write	Description
31:27	01110b	Read Only	PME_Support - This five bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(27) XXXX0b - PME# cannot be asserted from D0 bit(28) XXX1Xb - PME# can be asserted from D1 bit(29) XX1XXb - PME# can be asserted from D2 bit(30) X1XXXb - PME# can be asserted from D3hot bit(31) 0XXXXb - PME# cannot be asserted from D3cold
26	1b	Read Only	D2_Support - If this bit is a "1", this function supports the D2 Power Management State.
25	1b	Read Only	D1_Support - If this bit is a "1", this function supports the D1 Power Management State.
24	0b	Read Only	Dyn_Data_Support - Dynamic Data is not support.
23:22	00b	Read Only	Reserved
21	0b	Read Only	No Device Specific Initialization is required.
20	0b	Read Only	Auxiliary Power Source - Function does not support.
19	0b	Read Only	PME Clock - No PCI clock is required for this function to generate PME#.
18:16	001b	Read Only	Version - A value of 001b indicates that this function complies with the Revision 1.0 of the PCI Power Management interface Specification.
15:8	00h	Read Only	Next Item Pointer - No additional items in the Capabilities List.
7:0	01h	Read Only	ID - This field, when "01h" identifies the linked list item as being the PCI Power Management Registers.

Additional Power Management Register (Offset :A4h)

Bits	Default Value	Read/Write	Description			
31-24	00h	Read Only	Data - This register is used to report the state dependent data requested by the Data_Select field. The value of this register is scaledby the value reported by the Data_Scale field.			
			Value in Data_Select	Data Reported	Data_Scale Interpretation	Units/ Accuracy
			0	D0 Power consumed	0= Unknown 1= 0.1x 2= 0.01x 3= 0.001x	Watts
			1	D1 Power consumed		
			2	D2 Power consumed		
			3	D3 Power consumed		
			4	D0 Power dissipated		
			5	D1 Power dissipated		
			6	D2 Power dissipated		
			7	D3 Power dissipated		
			8	Common logic power consumption (Multi-function PCI devices, Function 0 only)		
			9-15	Reserved (function 0 of a multi-function device)	0= Unknown 1-3 = TBD	TBD
			8-15	Reserved (single function PCI devices and other functions (greater than function 0) within a multi-function device)	0= Unknown 1-3 = TBD	TBD
23:16	00h	Read Only	Bridge Support Extensions: Not support			
15	0b	Read/ Wr-Clear	PME_Status - This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. Writing a "1" to this bit will clear it and cause the function to stop asserting a PME# (if enabled). Writing a "0" has no effect. This bit defaults to "0" if the function does not support PME# generation from D3cold. If the function supports PME# from D3cold then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.			

14:13	00b	Read Only	Data_Scale - This two bit read-only field indicates the scaling factor to be used when interpreting the value of the Data register. The value & meaning of this field will vary depending on which data value has been selected by the Data_Select field.
12:09	0000b	Read/Write	Data_Select - This four bit field is used to select which data is to be reported through the Data register and Data_Scale field.
08	0b	Read/Write	PME_En - "1" enables the function to assert PME#. When "0" PME# assertion is disabled.
07:05	000b	Read Only	Reserved
04	0b	Read/Write	Ddata_PME_En - Dynamic Data PME Enable is not support.
03:02	00b	Read Only	Reserved
01:00	00b	Read/Write	PowerState - This two bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot

CardBus Socket Status & Control Register

These registers must be mapped into memory space to allow faster access than would be possible if they were in configuration space. All of these registers shall be initialized by PCIRST#.

Status Event Register (Offset: 00h)

The Status Event Register indicates a change in socket status has occurred. CSTCHG# is driven, by the controller, based on the bits in this register. These bits do not indicate what the change is, only that one has occurred. Software must read the Socket Present State Register for current status. All of the bits in this register can be cleared by writing a one to that bit. These bits can be set o a one by software through writing a one to the corresponding bit in the Force Register. All bits in this register are cleared by PCIRST#.

They may be immediately set again, if when coming out of CRST# the bridge finds the status unchanged (i.e. CSTSCHG reasserted or Card Detects still true). Software needs to clear this register before enabling interrupts. If it is not cleared, when interrupts are enabled an interrupt will be generated based on any bit set but not masked.

BIT POSITION	NAME	DESCRIPTION
0	CSTSCHG/ WAKEUP	Card Status Change and/or Wakeup bit. This bit indicates that the CSTSCHG and/or WAKEUP signal has been asserted. It only indicates the assertion event. It is not a reflection of the CSTSCHG bit from the card. It will be latched by the controller and must be explicitly cleared by the appropriate software. The status change interrupt, driven the controller, must be based on this event bit rather than the Present Value register. When a card is powered this bit indicates a status change and is driven continuously by the card. When a socket is powered down, this bit is a WAKEUP bit. A card might only drive it for 1 ms to limit drain on a battery. To be used in this manner a card must haven an external supply or battery. Deassertion of CSTSCHG is controlled by software or reset clearing the signal on the bus. Indicating that change would not be useful. This bit will not be set if an event is detected during the time period when the bridge has started the power up cycle of the socket but has not yet signaled a Power Up Complete interrupt. This prevents spurious signals form a card, during powerup, generating invalid events. This bit will be re-enabled when the Power Complete interrupt is generated. During the power down sequence the card is responsible for preventing glitches.
1-2	CCD1 & CCD2	Card Detects 1 and 2. Indicate a change has occurred in the corresponding Card Detect bit.
3	Power Cycle	The bridge has completed powering up the CardBus socket. The Present State register should be read to determine that the voltage requested was actually applied. The bridge will not allow an unsupported voltage to be applied to a CardBus card. This bit is meaningless when an 16-bit card is installed.
4-31	Reserved	

Status Mask Register (Offset: 04h)

This register gives software the ability to control what status change interrupts are generated by the bridge. If the Card Detect Changed bit is enabled at the time a card is removed, interrupt will be generated then this register is cleared automatically. This is to prevent spurious interrupts while cards are removed. If it is desired to have the bridge generate an interrupt at the time of a new cards insertion, software must again set the Card Detect Changed mask bit. This register is cleared by a PCIRST#.

BIT POSITION	NAME	DESCRIPTION
0	CSTSCHG/ WAKEUP	When set enables an interrupt based on the CSTSCHG signal being asserted by a CardBus card. This bit is meaningless when an 16-bit card is installed. CSTSCHG interrupts generated by 16-bit cards are controlled via registers in that IF's register space. Default = 0 (disabled).
1-2	Card Detect Changed	When set enables an interrupt when the bridge detects change. Default = 00 (disabled).
3	Power Cycle Complete	When set the bridge will generate an interrupt 256 cycles after powering up a socket. Default = 0 (disabled).
4-31	Reserved	

Present State Register (Offset: 08h)

The Socket Present State Register reflects the present value of the socket's status. Some of the bits in this register are merely reflections of interface signals while others are flags set to indicate a status change.

BIT POSITION	NAME	DESCRIPTION
0	CSTSCHG/ WAKEUP	Card Status Change bit. This bit reflects the current status of the CSTSCHG/WAKEUP pin on the CardBus interface.
1-2	CCD1# and CCD2#	Card Detects 1 and 2. Provide for detection of a PC card insertion/removal/presence. Also used by the bridge, in conjunction with CVS1 and CVS2, to determine card type (16-bit vs. CardBus). They are reflections of the CCD1 and CCD2 pins.
3	PowerCycle	When set indicates the interface is powered up. When cleared the socket is powered down. Set to zero by PCIRST#.
4	16-bit PC Card	When set indicates that the Card Detect state machine determined a PCMCIA card was inserted. This bit is cleared when another card is inserted that isn't 16-bit. This bit is set to zero by a PCIRST#.
5	CBCard	When set indicates that the Card Detect state machine determined a CardBus card was inserted. This bit is cleared when another card is inserted that isn't CardBus. This bit is set to zero by PCIRST#. NOTE: This bit and the 16-bit Card bit do not indicate that a card is installed. They only indicate what kind of card was last installed. The Card Detect bits indicate if a card is currently in the socket.
6	Interrupt	When set to one indicates the inserted card is driving its interrupt pin true. This bit is not a registered bit and its assertion/deassertion must follow the interrupt pin from the card.
7	NotACard	Indicates that an unsupported card is installed in the socket. The bridge will not allow power to be applied to the socket if this bit is set. Set to zero by PCIRST#.
8	DataLost	Indicates that a card was removed while the interface was active. Data may have been lost. Any data in the bridge's data buffers when this occurs is lost. Set to zero by PCIRST#. WHY: To allow software to fail in a graceful manner, if it chooses to, when this happens.
9	BadVccReq	Software attempted to apply an unsupported or incorrect voltage level to a socket. This bit is set to zero by PCIRST#.
10	5VCard	When set the card installed requires and/or supports 5.0V operation. This bit is set by the state machine used to detect card voltage requirements. This bit is set to zero by PCIRST#.
11	3V Card	When set the card installed requires and/or supports 3.3V operation. This bit is set by the state machine used to detect card voltage requirements. This bit is set to zero by PCIRST#.
12	XVCard	Unused. Returns 0.
13	YVCard	Unused. Returns 0.
14-27	Reserved	Return zero when read
28-31	Vcc Voltage Available	Indicates the Vcc voltages available for the sockets in this machine

Vcc Voltage Available

Bit #31	Bit #30	Bit #29	Bit #28
YV	XV	3V	5V

Force Register (Offset 0Ch)

The Force Register is a phantom register. Its bits are merely control bits. They are not registered and need no clearing. It provides software the ability to force various status and event bits in the bridge. This gives software the ability to test and restore status. Writing a one to a bit in this register sets the corresponding bit in the Socket Event Register and/or the Present State Register.

BIT POSITION	NAME	DESCRIPTION
0	CSTSCHG	Sets the Card Status Change bit in the Event Register. The Present State Register remains unchanged
1-2	Card Detect Changed	Sets the Card Status Change bit in the Event Register. The Present State Register remains unchanged
3	Power Up	Sets the PowerCycle bit in the Event Register. The Present State Register remains unchanged.
4	16-bit Card	Sets the 16-bit Card bit in the Present State Register. If a card is installed in the socket, writes to this bit are ignored.
5	CBCard	Sets the CBCard bit in the Present State Register. If a card is installed in the socket, writes to this bit are ignored.
6	Reserved	
7	NotACard	Sets the NotACard bit in the Present State Register. If a card is installed in the socket, writes to this bit are ignored.
8	Data Lost	This bit will cause the Data Lost bit to be set in the Present State Register.
9		BadVccReq - This bit will cause the BadVccReq bit in the Present State Register to be set.
10	5VCard	This bit will cause the 5VCard bit in the Present State Register to be set. Writes to this bit disables the bridge's ability to power up the socket. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or reset the card's supported voltages. The latter can be accomplished by forcing the CV Test bit. This is necessary to prevent software from applying an incorrect voltage to the bridge.
11	3VCard	This bit will cause the 3VCard bit in the Present State Register to be set. Writes to this bit disables the bridge's ability to power up the socket. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or reset the card's supported voltages. The latter can be accomplished by forcing the CV Test bit. This is necessary to prevent software from applying an incorrect voltage to the bridge.
12-13	Reserved	
14	CV Test	Causes the controller to test the VS and CCD lines to determine card type and voltages supported. This test is run automatically when a new card is inserted.
15-31	Reserved	

Control Register(Offset: 10h)

The Socket Control Register provides control of the socket's Vcc and Vpp. All bits in this register should be set to zero by PCIRST# and power removed from the socket

BIT POSITION	NAME	DESCRIPTION
0-1	Vpp Control	Used to switch the Vpp power using external Vpp control logic. The bridge has no knowledge of a card's Vpp voltage requirement. Software must determine the needed voltage from the card's CIS.
3	Unused	Unused - Returns zero when read.
4-6	VCC Control	Used to control the power to the PC Card via external control logic. The bridge determines the voltages that can be applied by decoding the CD and VS signals per the CardBus specification. Those bits and the voltages available in the system determine the correct Vcc options. The value written to this register must agree with the value needed to apply the correct value of Vcc. The bridge must not allow an incorrect VCC voltage to be applied to a socket. The voltages available are shown in the Status Register.
7	StopClock	When set causes the bridge to stop the CardBus clock (CCLK) using the CLKRUN# protocol. This allows software control of the CLKRUN# protocol in those systems that do not support CLKRUN# on the host side of the controller. Default is 0.
8-31	Unused	Returns zero when read.

Bit #2	Bit #1	Bit #0	VPP Requested
0	0	0	0V
0	0	1	12.0V
0	1	0	5.0V
0	1	1	3.3V
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Bit #6	Bit #5	Bit #4	Vcc Requested
0	0	0	0V
0	0	1	Reserved
0	1	0	5.0V
0	1	1	3.3V
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Socket Zoomed Video Control Register(Offset: 20h)

The Zoomed Video Control Register provide control of each socket zoomed video mode enable . All bits in this register should be set to zero by PCIRST# . This register bit 0 will directly reflect at bit 3 of Index Register 3A/7A.

BIT POSITION	NAME	DESCRIPTION
0	Zoomed Video	0: socket address lines are nomal. 1: socket address lines A[25:4] are High-Impedance IOIS16#, INPACK# and BVD2/SPKR# are ignored by the OZ6833 while in ZV Port mode.
31-1	Unused	Unused - Returns zero when read.

Socket Interrupt and MHPG DMA Control Register(Offset: 24h)

The Socket Interrupt and MHPG DMA Control Register provide control of each socket status change and CINT# interrupt enable. This register bit [4:0] will directly reflect at bit [4:0] of Index Register 3C/7C.

BIT POSITION	NAME	DESCRIPTION
2-0	MHPG DMA Channel #	Define the DMA channel number from 0h-7h
3	CINT# Enable	Bit is "0" indicates that when CardBus CINT# active will **not** generate the Interrupt Bit is "1" indicates that when CardBus CINT# active will generate the Interrupt **(Default)**
4	Status Change Interrupt Enable	Bit is "0" indicates that when Socket Status changes will **not** generate the Interrupt Bit is "1" indicates that when Socket Status changes will generate the Interrupt **(Default)**
31-5	Unused	Unused - Returns zero when read.

O₂MICRO MISC CONTROL Register (Offset: 28h)

This register bit [1:0] will directly reflect at bit [6:5] of Index Register 38/78.
This register bit [9:8] will directly reflect at bit [1:0] of Index Register 3B/7B.
This register bit [11:10] will directly reflect at bit [7:6] of Index Register 3B/7B.
This register bit [16] will directly reflect at bit [4] of Index Register 3D/7D.
This register bit [23:22] will directly reflect at bit [7:6] of Index Register 3D/7D.
This register bit [25:24] will directly reflect at bit [1:0] of Index Register 3E/7E.
This register bit [28:27] will directly reflect at bit [4:3] of Index Register 3E/7E

.BIT POSITION	NAME	DESCRIPTION
[1:0]	Pwrchip	**00 =>Reserved** **01 => parallel socket pwr** **10 => TI TPS2202IDF** **11 => SMBUS MAX1601**
[7:2]	Reserved	Return zero when read
[9:8]	System Interrupt Mode	These bits indicate the type of interrupt mode selected in PCI-Compatible interrupt mode 00 => PC/PCI interrupt mode 01 => Reserved 10 => PCI/Way interrupt mode 11 => PCI interrupt mode(Default)
10	WIN97 IRQ Support	Bit is "1", indicates CardBus 32 bit card is using PCI interrupt & PC 16 bit card using ISA Serial mode to support WIN97 Bit is "0", indicates Interrupt Mode is decided by system Interrupt Mode
11	ISA Legacy	Bit is "1", indicates ISA-legacy interrupt mode Bit is "0", indicates PCI-compatible interrupt mode(**Default**)
[15:12]	Unused	Unused - Returns zero when read.
16	PCI_FIFO	Bit is "1", indicates PCI side Word buffer enabled Bit is "0", indicates PCI side Dword buffer disabled
[17:21]	Unused	Unused - Returns zero when read.
22	MEM_POSTWR	Bit is "0" indicates that Cardbus bridge memory post write function disabled Bit is "1" indicates that Cardbus bridge memory post write function enabled
23	Buffer Enable	Bit is "0" indicates that CardBus bridge memory FIFO full buffer disabled Bit is "1" indicates that CardBus bridge memory FIFO full buffer Enabled
24	MHPG DMA MODE	"0" indicates that MHPG DMA Mode not enabled. "1" indicates that MHPG DMA MODE Enabled
25	SPKR_OUT Enable	"1" indicates that enable the output for pin SPKR_OUT(**Default)** "0" indicates that disable the output for pin SPKR_OUT
26	Reserved	
27	LED_OUT Enable	"1" indicates that enable the output for pin LED_OUT(**Default)** "0" indicates that disable the output for pin LED_OUT
28	SKTA_ACTV	Bit is "0" indicates LED_OUT/SKT_ACTV pin is Led_Out Bit is "1" indicates LED_OUT/SKT_ACTV pin is **SocketA_Activity** **SocketB_Activity pin refer to PCI Configuration Register 90h**
31-29	Unused	Unused - Returns zero when read.

ExCA REGISTERS

The ExCA registers implemented in the OZ6833 are registered compatible with Intel 82365SL-DF PCMCIA Controller .The OZ6833 provides two ways for accessing the ExCA-compatible register.

(1) Via the CardBus Socket/ ExCA Base Address Register - (Configuration offset : 10h) and mapped directly into memory address space. ExCA registers, offset by 800h
(2) Via the 16-bit PC Card Legacy Mode Base Address Register (Configuration offset : 44h)

PCI Memory Address Space

CardBus Socket/
ExCA Base Address Register
(function zero)
Base Address

Offset from Base

CardBus Socket Registers

00h

20h

800h   Socket A(0)

ExCA Socket Interface Registers

00h

3Fh   840h

16-Bit Legacy Register
(aliased between functions)
Base Address

Index Address Reg   ExCA Offset(00h-7Fh)

Index Data Reg   Data to/from ExCA Reg

CardBus Socket/
ExCA Base Address Register
(function one)
Base Address

CardBus Socket Registers

00h

20h

800h   Socket B(1)

ExCA Socket Interface Registers

00h

3Fh   840h

Index Register Table

All the registers', except index 00h/40h, default value are 00h.

Socket A Memory Offset	Socket A I/O Offset	Socket B Memory Offset	Socket B I/O Offset	Register Name
				GENERAL SETUP REGISTERS
800h	00h	800h	40h	Identification and Revision
801h	01h	801h	41h	Interface Status
802h	02h	802h	42h	Power and RESETDRV Control
804h	04h	804h	44h	Card Status Change
806h	06h	806h	46h	Address Window Enable
816h	16h	816h	56h	Card Detect and General Control Register
81Eh	1Eh	81Eh	5Eh	Global Control Register
				INTERRUPTS REGISTERS
803h	03h	803h	43h	Interrupt and General Control
805h	05h	805h	45h	Card Status Change Interrupt Configuration
				I/O REGISTERS
807h	07h	807h	47h	I/O Control
808h	08h	808h	48h	I/O Address 0 Start LOW Byte
809h	09h	809h	49h	I/O Address 0 Start HIGH Byte
80Ah	0Ah	80Ah	4Ah	I/O Address 0 Stop LOW Byte
80Bh	0Bh	80Bh	4Bh	I/O Address 0 Stop HIGH Byte
80Ch	0Ch	80Ch	4Ch	I/O Address 1 Start LOW Byte
80Dh	0Dh	80Dh	4Dh	I/O Address 1 Start HIGH Byte
80Eh	0Eh	80Eh	4Eh	I/O Address 1 Stop LOW Byte
80Fh	0Fh	80Fh	4Fh	I/O Address 1 Stop HIGH Byte
				MEMORY REGISTERS
810h	10h	810h	50h	System Memory Address 0 Mapping Start LOW Byte
811h	11h	811h	51h	System Memory Address 0 Mapping Start HIGH Byte
812h	12h	812h	52h	System Memory Address 0 Mapping Stop LOW Byte
813h	13h	813h	53h	System Memory Address 0 Mapping Stop HIGH Byte
814h	14h	814h	54h	Card Memory Offset Address 0 LOW Byte
815h	15h	815h	55h	Card Memory Offset Address 0 HIGH Byte
840h	17h	840h	57h	System Memory Address 0 Mapping Start Upper Byte
818h	18h	818h	58h	System Memory Address 1 Mapping Start LOW Byte
819h	19h	819h	59h	System Memory Address 1 Mapping Start HIGH Byte
81Ah	1Ah	81Ah	5Ah	System Memory Address 1 Mapping Stop LOW Byte
81Bh	1Bh	81Bh	5Bh	System Memory Address 1 Mapping Stop HIGH Byte
81Ch	1Ch	81Ch	5Ch	Card Memory Offset Address 1 LOW Byte
81Dh	1Dh	81Dh	5Dh	Card Memory Offset Address 1 HIGH Byte
841h	1Fh	841h	5Fh	System Memory Address 1 Mapping Start Upper Byte
820h	20h	820h	60h	System Memory Address 2 Mapping Start LOW Byte
821h	21h	821h	61h	System Memory Address 2 Mapping Start HIGH Byte
822h	22h	822h	62h	System Memory Address 2 Mapping Stop LOW Byte
823h	23h	823h	63h	System Memory Address 2 Mapping Stop HIGH Byte
824h	24h	824h	64h	Card Memory Offset Address 2 LOW Byte
825h	25h	825h	65h	Card Memory Offset Address 2 HIGH Byte
826h	26h	826h	66h	Reserved
842h	27h	842h	67h	System Memory Address 2 Mapping Start UPPER Byte
828h	28h	828h	68h	System Memory Address 3 Mapping Start LOW Byte
829h	29h	829h	69h	System Memory Address 3 Mapping Start HIGH Byte
82Ah	2Ah	82Ah	6Ah	System Memory Address 3 Mapping Stop LOW Byte
82Bh	2Bh	82Bh	6Bh	System Memory Address 3 Mapping Stop HIGH Byte
82Ch	2Ch	82Ch	6Ch	Card Memory Offset Address 3 LOW Byte
82Dh	2Dh	82Dh	6Dh	Card Memory Offset Address 3 HIGH Byte
82Eh	2Eh	82Eh	6Eh	Reserved
843h	2Fh	843h	6Fh	System Memory Address 3 Mapping Start UPPER Byte
830h	30h	830h	70h	System Memory Address 4 Mapping Start LOW Byte
831h	31h	831h	71h	System Memory Address 4 Mapping Start HIGH Byte
832h	32h	832h	72h	System Memory Address 4 Mapping Stop LOW Byte
833h	33h	833h	73h	System Memory Address 4 Mapping Stop HIGH Byte
834h	34h	834h	74h	Card Memory Offset Address 4 LOW Byte
835h	35h	835h	75h	Card Memory Offset Address 4 HIGH Byte
836h	36h	836h	76h	Reserved
837h	37h	837h	77h	Reserved
838h	38h	838h	78h	O$_2$ Micro Mode Control A
839h	39h	839h	79h	O$_2$ Micro Mode Control B
83Ah	3Ah	83Ah	7Ah	O$_2$ Micro Mode Control C
83Bh	3Bh	83Bh	7Bh	O$_2$ Micro Mode Control D
83Ch	3Ch	83Ch	7Ch	MHPG DMA Register
83Dh	3Dh	83Dh	7Dh	FIFO Enable Register
83Eh	3Eh	83Eh	7Eh	O$_2$Micro Mode Control E
844h	3Fh	844h	7Fh	System Memory Address 4 Mapping Start UPPER Byte

General Setup Registers

IDENTIFICATION AND REVISION REGISTER (READ ONLY)

Socket A: Index Value (Base + 00h)
Socket B: Index Value (Base + 40h)

The Identification and Revision register is used by the system software to determine the type of PC Cards supported, and to identify what version of the OZ6833 is present. System software reads the identification and revision Register and then compares the result value against existing revision numbers (83h for Intel365SL Step B; 84h for Intel365SL Step C; and 87h for OZ6833; this register default can be programmed by O_2Micro Control B Register)

BIT POSITION	NAME	DESCRIPTION
[7:6]	OZ6833 Interface ID bit [1:0]	These bits indicate the type of PC Cards supported by the OZ6833 at the particular socket. **ID[1] ID[0] Interface** 0 0 I/O Only 0 1 Memory Only 1 0 Memory & I/O 1 1 Reserved **NOTE:** These bits will read back as 10
[5:4]	Reserved	These bits will be read back as "0"s
[3:0]	OZ6833 Revision bit [3:0]	These four bits indicate the current revision level of the OZ6833. The revision code will be 0010.

INTERFACE STATUS REGISTER (READ ONLY)

Socket A: Index Value (Base + 01h)
Socket B: Index Value (Base + 41h)

The Interface Status Register provides the current status of the PC Card socket interface signals.

BIT POSITION	NAME	DESCRIPTION
7	Reserved	Read as "0".
6	PC Card Power Active	Indicates the current power status of the socket. If bit is set to "0", power to the socket is turned off (Vcc, Vpp1, and Vpp2 will not be actively driven by the proper voltage supply). If bit is set to "1", power is provided to the socket (Vcc = 5V and Vpp1 and Vpp2 are set according to bits 3-0 in the power control register).
5	Ready/Busy#	Indicates the ready condition of the PC Memory Card. If bit is set to "1", the PC Card is ready to accept a new data transfer. If bit is "0", the PC Card is busy processing a previous command, or performing initialization for IO Card, this bit is default to HIGH.
4	Memory write protect	Bit value is the logic level of the **WP** signal on the memory PC Card interface. This bit is set to "0" when WP = "0". However, memory write access to the slot will not be blocked unless the write protect bit in the associated Card Memory Offset Address Register HIGH byte register is set to "1".
[3:2]	Card Detect 2 and 1	Together they indicate whether card is present at the socket and fully seated. Bits are set to ones if the **CD1#, CD2#** signal on the PC Card interface are active. Bits are set to "0" if the **CD1#, CD2#** signals on the PC Card interface is inactive.
[1:0]	Battery Voltage Detect 2 and 1	**BVD1 BVD2 STATUS** 0 0 Battery Dead 0 1 Battery Dead 1 0 Warning 1 1 Battery Good For I/O PC Cards, bit "0" indicates the current status of the (BVD1/STSCHG#) signal from the PC Card . For I/O PC Cards bit 0 indicates the current state **SPKR#** signal from the PC Card. Refer to interrupt General Control Register (03h, 43h) bit 7 for more details.

POWER AND RESETDRV CONTROL REGISTER (READ/WRITE)

Socket A: Index Value (Base + 02h)
Socket B: Index Value (Base + 42h)

This register controls the PC card power and resetting of OZ6833 registers.

BIT POSITION	NAME	DESCRIPTION
7	Output Enable	If this bit is set to "0", the PC card outputs listed below are tri-stated. A[25:0], CE2#. CE1#, IORD#, IOWR#, OE#, REG#, RESET, WE#
6	Reserved	
5	Auto Pwr Switch Enable	If bit is set to "0", automatic socket power switching based on card detects is disabled. If bit is set to "1", automatic socket power switching based on card detects is enabled. Automatic socket power switching function controls the VCC_3#, VCC_5#, VPP_VCC and VPP_PGM output pins.
4	PC card Power Enable	If bit is set to "0", all power to the PC card is disabled. When bit is set to "1", power will be supplied to the sockets through VCC_3# and VCC_5# pin depending on the type of voltage the card needs.
3	Vcc3.3V	This bit determines which output pin is to be used to enable Vcc power to the socket when card power is to be applied; it is used in conjunction with bit 5-4 the **Power Control** register. **0** - Vcc_5 activated when card power is to be applied. **1** - Vcc_3 activated when card power is to be applied.
2	Reserved	This bit will be read back as"0"s.

[1:0]	Vpp Control Bits	These bits control the VPP_VCC and VPP_PGM output pins of the OZ6833.
		
		[1] [0] VPP_PGM VPP_VCC PCMCIA Intended Socket Function
		  0 0 Inactive LOW Inactive LOW Zero volts to socket Vpp1 pin
		  0 1 Inactive LOW Active HIGH Selected card Vcc to socket Vpp1 pin
		  1 0 Active HIGH Inactive LOW +12V to socket Vpp1 pin
		  1 1 Inactive LOW Inactive LOW Zero volts to socket Vpp1 pin

The table below describes the slot power control function.

PWRGOOD Level	Power Control Register		CD1# and CD2# Active LOW	Interface Status Register	VCC_3# and VCC_5# Levels	VPP1_PGM and VPP1_VCC Levels
	Bit 4 (VCC Power)	Bit 5 (Auto Power)		Bit 6 (Card Power On)		
LOW	X	X	X	0	Inactive HIGH	Inactive HIGH
HIGH	0	X	X	0	Inactive HIGH	Inactive HIGH
HIGH	1	0	X	1	Activated with supply voltage depend on VS# input pin.	Activated with supply VPP voltage depend on Power Control register bits "1" and "0".
HIGH	1	1	No	0	Inactive HIGH	Inactive HIGH
HIGH	1	1	Yes	1	Activated with supply voltage depend on VS# input pin.	Activated with supply VPP voltage depend on Power Control register bits "1" and "0"

CARD STATUS CHANGE REGISTER (READ/WRITE)

Socket A: Index Value (Base + 04h)
Socket B: Index Value (Base + 44h)

This register contains the status of the sources for the card status change interrupts. These sources can be enabled to generate a card status change interrupt by setting the corresponding bit in the Card Status Change Interrupt Configuration Register. The bits in this register will be read back as "0", when the Card Status Enable bits are set to "0" in the Card Status Change Interrupt Configuration Register for the various sources of the card status change interrupts.

If the Explicit write Back Card Status Change Acknowledge bit is set in the Global Control Register, the acknowledgment of sources for the card status change interrupt will be done by writing back "1" to the appropriate bit in the Card Status Change register that was read as a "1". Once acknowledged, that particular bit in the Card Status Change register will be read back as "0". The interrupt signal caused by card status change, if enabled on a system IRQ line, will be active until all of the bits in this register are"0".

If the Explicit write Back Card Status Change Acknowledge bit is not set, the card status change interrupt when enabled on a system IRQ line, will remain active until the Card Status Change register is read. The read operation to the Card Status Change Register will reset all the bits in that register.

In the case that there are two or more card status change interrupts pending, and a card status change interrupt condition occurs while serving one source of card status change, the OZ6833 will not generate a second interrupt pulse.

Therefore, in explicit write back acknowledge mode, the Host System interrupt service routine needs to acknowledge each Card Status Change Interrupt source by writing "1"s to the respective bits in the Card Status Change Register. While in the standard acknowledge mode, the SW interrupt service routine must first read the Card Status Change register to store all the card status change sources and service them in terms.

In both modes, the Interrupt Service Routine needs the Card Status Change register to make sure that all interrupt requests are serviced before emitting the service routines.

NOTE: bit descriptions in parenthesis indicate valid signals after the interface is configured for I/O type PC cards.

BIT POSITION	NAME	DESCRIPTION
[7:5]	Reserved	These reserved bits always read "0".
4	Reserved	Read as "0".
3	Card detect Change	Bit is set to "1" when a change has been detected on either the **CD1#** or **CD2#** signals.
2	Ready Change	Bit is set to "1" when a LOW to HIGH transition has been detected on the **READY/BUSY#** signal indicating that the memory PC Card is ready to accept a new data transfer. Bit reads "0" for I/O Cards
1	Battery Warning	Bit is set to "1"when a battery warning condition has been detected. Bit reads "0" for I/O PC Cards.
0	Battery Dead (VD1/STSCHG#)	For memory PC Cards, bit is set to "1" when a battery dead condition has been detected. For I/O PC Cards, bit is set to "1" if ring indicate enable bit in the Interrupt and General Control register is set to "0" and the (**VD1/STSCHG#**) signal from the I/O PC Card has been pulled LOW. The system software then has to read the status change register in the PC Card to determine the cause of the status change signal (**STSCHG#).** This bit reads "0" for I/O PC Cards if the ring indicate enable bit in the Interrupt and General Control register is set to "1".

ADDRESS WINDOW ENABLE REGISTER (READ/WRITE)

Socket A: Index Value (Base + 06h)
Socket B: Index Value (Base + 46h)

This register controls the enabling of the memory and I/O mapping windows to the PC Card memory or I/O space.
For CS# controlled power-down mode to function properly, all the memory I/O window enable bits in this register need to be set to "0" before the OZ6833 enters the power-down mode.

BIT POSITION	NAME	DESCRIPTION
7	I/O Window 1 Enable	If bit is set to "0", an I/O access within the I/O address 1 window will inhibit the card enable signals to the PC Card. If bit is set to "1", an I/O access within the I/O address 1 window will generate the card enables to the PC Card. I/O accesses pass addresses from the system bus directly through to the PC Card. *The start and stop register pairs must all be set to the desired window values before setting bit to "1".*
6	I/O Window 0 Enable	If bit is set to "0", an I/O access within the I/O address 0 window will inhibit the card enable signals to the PC Card. If bit is set to "1", an I/O access within the I/O address 0 window will generate the card enables to the PC Card. I/O accesses pass addresses from the system bus directly through to the PC Card. *The start and stop register pairs must all be set to the desired window values before setting bit to "1".*
5	MEMCS16# Decode A23-A12	If this bit is set to "0", **MEMCS16#** is generated from a decode of the system (ISA) address lines A23-A17 only. This means that at a minimum, a 128K block of system (ISA) memory address space is set aside as 16-bit memory only. If this bit is set to a"1", **MEMCS16#** is generated from decode of the system (ISA address lines A23-A12).
4	Memory Window 4 Enable	If bit is set to "0", a memory access within the memory address 4 window will inhibit the card enable signals to the PC Card. If bit is set to "1", a memory access within the system memory address 4 window will generate the card enables to the PC Card. *The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to* "1". When bits is set to "1" and the system address is within the window, the computed address will be generated to the PC Card.
3	Memory Window 3 Enable	If bit is set to "0", a memory an I/O access within the memory address 3 window will inhibit the card enable signals to the PC Card. If bit is set to "1", a memory access within the system memory address 3 window will generate the card enables to the PC Card. *The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to* "1". When bits is set to "1" and the system address is within the window, the computed address will be generated to the PC Card.
2	Memory Window 2 Enable	If bit is set to "0", a memory access within the memory address 2 window will inhibit the card enable signals to the PC Card. If bit is set to "1", a memory access within the system memory address 2 window will generate the card enables to the PC Card. *The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to* "1". When bits is set to "1" and the system address is within the window, the computed address will be generated to the PC Card.
1	Memory Window 1 Enable	If bit is set to "0", a memory access within the memory address 1 window will inhibit the card enable signals to the PC Card. If bit is set to "1", a memory access within the system memory address 1 window will generate the card enables to the PC Card. *The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to* "1". When bits is set to "1" and the system address is within the window, the computed address will be generated to the PC Card.
0	Memory Window 0 Enable	If bit is set to "0", a memory access within the memory address 0 window will inhibit the card enable signals to the PC Card. If bit is set to"1", a memory access within the system memory address 1 window will generate the card enables to the PC Card. *The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to* "1". When bits is set to "1" and the system address is within the window, the computed address will be generated to the PC Card.

GLOBAL CONTROL REGISTER (READ/WRITE)

Socket A: Index Value (Base + 1Eh)
Socket B: Index Value (Base + 5Eh)

This register is not duplicated per slot. Thus, this register can be accessed from either the slot A or slot B index.

BIT POSITION	NAME	DESCRIPTION
[7:4]	Reserved	These bits are reserved.
3	IRQ14 Pulse Mode Enable	Setting this bit to a "1" and bit 1 (level mode interrupt enable bit) to "0" will enable the OZ6833 to use IRQ14 to support PC card with pulse mode interrupt on IREQ# while other IRQ's are still supporting edge-trigger interrupts (from either card status change interrupts, or PC card IREQ#). If bit 1 is set to "1", then this bit has no effect.
2	Explicit Write Back Card Status Change Acknowledge	Setting this bit to a "1", will require an explicit write of a "1" to the Card status change Register bit which indicates an interrupting condition. When this bit is set to "0" (default state), the card status change interrupt is acknowledged by reading the Card Status Change Register, and the register bits are cleared upon a read.
1	Level Mode Interrupt Enable	If this bit is set to "1", then all the **IRQ** outputs are configured to be active LOW level mode interrupts. In this mode, an **IRQ** will remain tristated until there is either a card status change interrupt or an I/O card interrupt steered to that particular IRQ and active, at which time the **IRQ** output will go LOW. For the interrupt caused by the IREQ# active (LOW) from a PC Card, IRQ will remain LOW until IREQ# become inactive, then **IRQX** will be deasserted. For the interrupt caused by the card status change, it will remain LOW until interrupt is acknowledged (serviced). Once serviced the **IRQ** output will go from LOW to tristate.

If this bit is set to its default state of "0", the **IRQ** outputs will be configured to be LOW to HIGH edge triggered interrupts. In this mode, the IRQs will remain tristated until the particular IRQ is enabled, at which time the IRQ output will go LOW. The output will stay LOW until there is a card status change interrupt or I/O card interrupt which will cause the **IRQ** output to HIGH. For the interrupt caused by the IREQ# active (LOW) from a PC Card, IRQx will remain HIGH until IREQ# becomes inactive, then IRQ will be LOW again. For the interrupt caused by the card status change, it will remain HIGH until interrupt is acknowledged (serviced), then goes LOW. In either case, IRQs will then remain LOW until they are disabled (through interrupt and general control register). When disabled, IRQ will become tristated. |
| 0 | Power Down | When it is set to "1", and all I/O memory windows are disabled, and CS# signal is driven to inactive HIGH, the OZ6833 enters the CS# controlled power-down. During CS# controlled power-down, all OZ6833's internal registers are inaccessible, outputs are disabled, and the OZ6833 is at minimum power consumption level. IRQ's and RI_OUT# will still be active to monitor the card detect, and RI# status for resume indication. |

CARD DETECT AND GENERAL CONTROL REGISTER (READ/WRITE)

Socket A: Index Value (Base + 16h)
Socket B: Index Value (Base + 56h)

BIT POSITION	NAME	DESCRIPTION
[7:6]	Reserved	These bits are reserved.
5	Software card detect Interrupt	If the Card Detect enable bit is set to "1" in the Card Status Change Interrupt Configuration Register, then writing a "1" to this bit will cause a card detect card status change interrupt for the associated slot. The functionality and acknowledgment of this software interrupt will work the same way as the hardware generated interrupt.
		NOTE: The functionality of the hardware card detect card status change interrupt will not be affected. The previous state of the CD1# and CD2# inputs will be latched, such that while a S/W card detect card change interrupt occurs and is serviced, and a change from the previous state occurs on the CD1# and CD2# inputs, a H/W card detect card status change interrupt will be generated.
		If the Card Detect Enable bit is set to "0" in the Card Status Change Interrupt Configuration Register, then writing a "1" to the S/W Card Detect Interrupt bit has no effect.
		The S/W Card Detect Interrupt bit will always read back as a "0".
4	Card Detect Resume Enable	The default state of this bit is "0". If this bit is set to "1", then once a card detect change has been detected on the **CD1#** and **CD2#** inputs, the **RI_OUT#** output will go from HIGH to LOW and the Card Detect Change bit in the Card Status Change Register will be set to "1". The **RI_OUT#** output will remain LOW until either a read or a write of "1" to the Card Detect Change bit in the Card Status Change register , (acknowledge cycle) which will cause the Card Detect Change bit to be cleared and the RI_OUT# output to go from LOW to HIGH. The Card Detect Enable bit must be set in the Card Status Change Interrupt Configuration Register in order to generate the RI_OUT#.
		If the card status change is routed to the IRQ signals, the setting of Card Detect Resume Enable bit to "1" will prevent IRQ signal from going active as a result of card status change. Once the resume software has detected a card detect change interrupt from **RI_OUT#(**by reading the Card status Change register), the software should initiate a software card detect change so the card detect change condition will generate active interrupt on the IRQ signals (depending on the active configuration).
		If this bit is set to "0", then the card detect resume functionality is disabled. This means that the **RI_OUT#** output will not go LOW due to a card detect change.
		The **RI_OUT#** output will be the logical AND of all the active LOW sources for ring indicate output including the **RI#** inputs from slot A and slot B and the card detect changes on **CD1#, CD2#** from both slots.
3	Reserved	**Read as "0".**
2	Reserved	Read as "0".
0	16-Bit Memory Delay Inhibit	The default state of this bit is "0". **This is not programmable on a per window basis.** If it is set to "0" and a system memory window is set up to be 16-bit by setting the Data Size bit in the System Memory Address Mapping Start HIGH Byte Register to "1", the falling edge of the control strobes WE# and OE# for the corresponding slot will be delayed synchronously by SYSCLK. The falling edge of the control strobes will be generated from the first falling edge of SYSCLK after the falling edge of MEMW# or MEMR# gated by a valid system memory window decode. The rising edge of the control strobes will be generated from the rising edge of MEMW# or MEMR#.
		If the 16-bit Memory Delay Inhibit is set to "1" and system memory window is set up to be 16-bit, the control strobes WE# and OE# for the corresponding slot will not be synchronously delayed by SYSCLK.

Index

(Base + Slot A/Slot B)

Base + 03h/43h	Interrupt and General Control
Base + 06h/46h	Address Window Enable **(Except 'MEMCS16# Decode A23-A12 ' bit)**
Base + 07h/47h	I/O Control
Base + 08h/48h	I/O Address 1 Start LOW Byte
Base + 09h/49h	I/O Address 1 Start HIGH Byte
Base + 0Ah/4Ah	I/O Address 1 Stop LOW Byte
Base + 0Bh/4Bh	I/O Address 1 Stop HIGH Byte
Base + 0Ch/4Ch	I/O Address 2 Start LOW Byte
Base + 0Dh/4Dh	I/O Address 2 Start HIGH Byte
Base + 0Eh/4Eh	I/O Address 2 Stop LOW Byte
Base + 0Fh/4Fh	I/O Address 2 Stop HIGH Byte
Base + 10h/50h	System Memory Address 0 Mapping Start LOW Byte
Base + 11h/51h	System Memory Address 0 Mapping Start HIGH Byte
Base + 12h/52h	System Memory Address 0 Mapping Stop LOW Byte
Base + 13h/53h	System Memory Address 0 Mapping Stop HIGH Byte
Base + 14h/54h	Card Memory Offset Address 0 LOW Byte
Base + 15h/55h	Card Memory Offset Address 0 HIGH Byte
Base + 18h/58h	System Memory Address 1 Mapping Start LOW Byte
Base + 19h/59h	System Memory Address 1 Mapping Start HIGH Byte
Base + 1Ah/5Ah	System Memory Address 1 Mapping Stop LOW Byte
Base + 1Bh/5Bh	System Memory Address 1 Mapping Stop HIGH Byte
Base + 1Ch/5Ch	Card Memory Offset Address 1 LOW Byte
Base + 1Dh/5Dh	Card Memory Offset Address 1 HIGH Byte
Base + 20h/60h	System Memory Address 2 Mapping Start LOW Byte
Base + 21h/61h	System Memory Address 2 Mapping Start HIGH Byte
Base + 22h/62h	System Memory Address 2 Mapping Stop LOW Byte
Base + 23h/63h	System Memory Address 2 Mapping Stop HIGH Byte
Base + 24h/64h	Card Memory Offset Address 2 LOW Byte
Base + 25h/65h	Card Memory Offset Address 2 HIGH Byte
Base + 28h/68h	System Memory Address 3 Mapping Start LOW Byte
Base + 29h/69h	System Memory Address 3 Mapping Start HIGH Byte
Base + 2Ah/6Ah	System Memory Address 3 Mapping Stop LOW Byte
Base + 2Bh/6Bh	System Memory Address 3 Mapping Stop HIGH Byte
Base + 2Ch/6Ch	Card Memory Offset Address 3 LOW Byte
Base + 2Dh/6Dh	Card Memory Offset Address 3 HIGH Byte
Base + 30h/70h	System Memory Address 4 Mapping Start LOW Byte
Base + 31h/71h	System Memory Address 4 Mapping Start HIGH Byte
Base + 32h/72h	System Memory Address 4 Mapping Stop LOW Byte
Base + 33h/73h	System Memory Address 4 Mapping Stop HIGH Byte
Base + 34h/74h	Card Memory Offset Address 4 LOW Byte
Base + 35h/75h	Card Memory Offset Address 4 HIGH Byte

Interrupt Registers

INTERRUPT AND GENERAL CONTROL REGISTER (READ/WRITE)

Socket A: Index Value (Base + 03h)
Socket B: Index Value (Base + 43h)

The Interrupt and General Control Register controls the interrupt steering for the PC card I/O interrupt as well as general control of the OZ6833.

BIT POSITION	NAME	DESCRIPTION
7	Ring Indicate Enable	If bit is set to "1" and the PC card Type bit (Bit 5), is set to "1" (I/O PC Card), the (VD1/STSCHG#) signal from the I/O PC Card is used as a ring indicator signal and is passed through to the RI_OUT# output pin of the OZ6833. this function will still work when the OZ6833 is powered at 3.3V as long as the DC conditions for 3.3V operation are met. If bit is set to "0" and the PC Card type bit is set to "1" (I/O PC Card) , the (**VD1/STSCHG#)** signal from the I/O PC Card is used as the status change signal (**STSCHG#).** The current status of the signal is then available to be read from the Interface status Register (01H) and this signal can be configured as a source for the card status change interrupt. The ring indicate enable bit has no function when the PC Card type bit is set to "0" (memory PC Card). Bit7 Bit5 Function 0 0 No Function 0 1 STSCHG# 1 0 No Function 1 1 RI# --> RI_OUT#
6	PC Card RESET#	This is software reset to the PC Card. Setting bit to "0" activates the **RESET** signal to the PC Card. The **RESET** signal will remain active until bit is set to "1".
5	PC Card Type (Memory or I/O)	Setting bit to "1" selects an I/O PC Card which enables the PC Card interface multiplexed for routing of PC Card I/O signals. Setting bit to "0" selects a Memory PC Card.
4	Reserved	Read as "0"
[3:0]	IRQ Level Selection (I/O cards Only)	PC card IREQ# Interrupt Steering Table These bits select the redirection of the PC Card interrupt. IRQ IRQ IRQ IRQ Interrupt Bit 3 Bit 2 Bit 1 Bit 0 Request Level 0 0 0 0 IRQ Not selected 0 0 0 1 Reserved 0 0 1 0 Reserved 0 0 1 1 IRQ3 Enabled 0 1 0 0 IRQ4 Enabled 0 1 0 1 IRQ5 Enabled 0 1 1 0 Reserved 0 1 1 1 IRQ7 Enabled 1 0 0 0 Reserved 1 0 0 1 IRQ9 Enabled 1 0 1 0 IRQ10 Enabled 1 0 1 1 IRQ11 Enabled 1 1 0 0 IRQ12 Enabled 1 1 0 1 Reserved 1 1 1 0 IRQ14 Enabled 1 1 1 1 IRQ15 Enabled

CARD STATUS CHANGE INTERRUPT CONFIGURATION REGISTER (READ/WRITE)

Socket A: Index Value (Base + 05h)
Socket B: Index Value (Base + 45h)

This register controls interrupt steering of the card status change interrupt and the card status change interrupt enables.

BIT POSITION	NAME	DESCRIPTION
[7:4]	IRQs	Interrupt Steering for the Card Status Change Interrupt See Card Status Change Interrupt Steering table for the routing of card status change interrupts. INTR# Enable Bit (Interrupt & Gen Cntl Reg) / IRQ Bit 3 / IRQ Bit 2 / IRQ Bit 1 / IRQ Bit 0 / Interrupt Request Level 0 0 0 0 0 IRQ Not Selected 0 0 0 0 1 Reserved 0 0 0 1 0 Reserved 0 0 0 1 1 IRQ3 Enabled 0 0 1 0 0 IRQ4 Enabled 0 0 1 0 1 IRQ5 Enabled 0 0 1 1 0 Reserved 0 0 1 1 1 IRQ7 Enabled 0 1 0 0 0 Reserved 0 1 0 0 1 IRQ9 Enabled 0 1 0 1 0 IRQ10 Enabled 0 1 0 1 1 IRQ11 Enabled 0 1 1 0 0 IRQ12 Enabled 0 1 1 0 1 Reserved 0 1 1 1 0 IRQ14 Enabled 0 1 1 1 1 IRQ15 Enabled
3	Card Detect Enable	Setting bit to "1" enables a card status change interrupt when a change has been detected on the CD1# and CD2# signals. Setting bit to "0" disables the generation of a card status change interrupt when the CD1#, CD2# signal change state.
2	Ready Enable	Setting bit to "1" enables a card status change interrupt when a LOW to HIGH transition has been detected on the Read/Busy# signal. Setting bit to "0" disables the generation of a card status change interrupt when a LOW to HIGH transition has been detected on the Read/Busy# signal. Bit is ignored when the interface is configured for I/O PC cards.
1	Battery Warning Enable	Setting bit to "1" enables a card status change interrupt when a battery warning condition has been detected. Setting bit to "0" disables the generation of a card status change interrupt when a battery warning condition has been detected.
0	Battery Dead Enable (STSCHG#)	For memory PC cards, setting bit to "1" enables a card status change interrupt when a battery dead condition has been detected. For I/O PC cards, setting bit to "1" enables OZ6833 to generate a card status change interrupt if the (STSCHG#/RI#) signal has been pulled LOW by I/O PC card, assuming that the ring indicate enable bit in the Interrupt and General Control Register is set to "0". Setting bit to "0" disables the generation of the card status change interrupt. Bit is ignored when the interface is configured for I/O PC cards and the Ring Indicate Enable bit in the Interrupt and General Control register is set to "1".

I/O Registers

I/O CONTROL REGISTER (READ/WRITE)

Socket A: Index Value (Base + 07h)
Socket B: Index Value (Base + 47h)

BIT POSITION	NAME	DESCRIPTION
7	I/O Window 1 Wait State	If this bit is set to "1" , 16-bit system accesses occur with 1 wait state (4 SYSCLKs). Standard 16-bit I/O cycle completes in 3 SYSCLKs with IOCHRDY HIGH.
6	I/O Window 1 ZeroWait State	If bit is set to 1, 8-bit system I/O accesses completes in 3 SYSCLKs, with ZEROWS# signal asserted to the system bus. If bit is set to "0", the 8-bit system I/O access will complete in 6 SYSCLKs when PC card asserts no WAIT# signal, or more when WAIT# signal is asserted (cause IOCHRDY deasserted). The WAIT# signal will override this bit. Bit has no meaning for 16-bit I/O access. Such access will always occur with either 3 SYSCLK standard cycle when WAIT# is not active, or more when WAIT# is active, or Bit 7 is set.
5	I/O Window 1 IOCS16# Source	If bit is set to "0", the OZ6833 generates **IOCS16#** based on the value of the data size bit. If bit is set to "1", the OZ6833 generates **IOCS16#** based on the **IOIS16#** signal from the PC Card and data size bit is ignored.
4	I/O Window 1 Data Size	A "0" selects an 8-bit I/O data path to the PC Card, and a "1" selects a 16-bit I/O data path to the PC Card.
3	I/O Window 0 Wait State	Same as bit 7, but for I/O Window 0 .
2	I/O Window 0 ZeroWait State	Same as bit 6, but for I/O Window 0 .
1	I/O Window 0 IOCS16# Source	Same as bit 5, but for I/O Window 0 .
0	I/O Window 0 Data Size	Same as bit 4, but for I/O Window 0 .

I/O ADDRESS 1 START LOW BYTE REGISTER (READ/WRITE)

Socket A: Index (Base + 08h)
Socket B: Index (Base + 48h)

This register contains the low order address bits used to determine the start address of I/O address window 0.
This provides a minimum 1 byte window for I/O address window 0 .

BIT POSITION	NAME	DESCRIPTION
[7:0]	Address [7:0]	I/O Window 0 Start Address A7:A0

I/O ADDRESS 1 START HIGH BYTE REGISTER (READ/WRITE)

Socket A: Index (Base + 09h)
Socket B: Index (Base + 49h)

This register contains the high order address bits used to determine the start address of I/O address window 0.

BIT POSITION	NAME	DESCRIPTION
[7:0]	Address [15:8]	I/O Window 0 Start Address A15:A8

I/O ADDRESS 1 STOP LOW BYTE REGISTER (READ/WRITE)

    Socket A: Index (Base + 0Ah)
    Socket B: Index (Base + 4Ah)

This register contains the high order address bits used to determine the stop address of I/O address window 0.
This provides a minimum 1 byte window for I/O address window 0 .

NOTE : Do not attempt to overlay the I/O window over the top of the OZ6833 registers. This will cause the OZ6833 access type to change.

BIT POSITION	NAME	DESCRIPTION
[7:0]	Address [7:0]	I/O Window 0 Stop Address A7:A0

I/O ADDRESS 1 STOP HIGH BYTE REGISTER (READ/WRITE)

    Socket A: Index (Base + 0Bh)
    Socket B: Index (Base + 4Bh)

This register contains the high order address bits used to determine the stop address of I/O address window 0.

BIT POSITION	NAME	DESCRIPTION
[7:0]	Address [15:8]	I/O Window 0 Start Address A15:A8

I/O ADDRESS 2 START LOW BYTE REGISTER (READ/WRITE)

    Socket A: Index (Base + 0Ch)
    Socket B: Index (Base + 4Ch)

This register contains the low order address bits used to determine the start address of I/O address window 1.
This provides a minimum 1 byte window for I/O address window 1 .

BIT POSITION	NAME	DESCRIPTION
[7:0]	Address [7:0]	I/O Window 1 Start Address A7:A0

I/O ADDRESS 2 START HIGH BYTE REGISTER (READ/WRITE)

    Socket A: Index (Base + 0Dh)
    Socket B: Index (Base + 4Dh)

This register contains the high order address bits used to determine the start address of I/O address window 1.

BIT POSITION	NAME	DESCRIPTION
[7:0]	Address [15:8]	I/O Window 1 Start Address A15:A8

Memory Registers

SYSTEM MEMORY ADDRESS 0 MAPPING START LOW BYTE REGISTER (READ/WRITE)

Socket A: Index (Base + 10h)
Socket B: Index (Base + 50h)

These registers contain the low order address bits used to determine the start address of the corresponding system memory address mapping window. This provides a minimum memory mapping window of 4 Kbytes.

A memory PC Card is selected when the following conditions are satisfied :

1. The system memory address mapping window is enabled ;
2. The (ISA) system memory address is greater than or equal to the system memory address mapping start register A23:A12 (high and low byte) ;
3. The (ISA) system memory address is less than or equal to the system memory address mapping stop register
A23:A12 (high and low byte).

The system memory address mapping windows can all be configured by software to be independently used, or used in concert to perform mapping for special memory mapping requirements, like LIM/EMS (Lotus-Intel-Microsoft/Extended Memory Specification) or XIP (Execute in Place) .

NOTE : A memory window can not be set up below the first 64K of address space.

BIT POSITION	NAME	DESCRIPTION
[7:0]	Address [19:12]	System Memory Window Start Address A19:A12

SYSTEM MEMORY ADDRESS 0 MAPPING START HIGH BYTE REGISTER (READ/WRITE)

Socket A: Index (Base + 11h)
Socket B: Index (Base + 51h)

These registers contain the high order address bits used to determine the start address of the corresponding system memory address mapping window. Each system memory window has a data path size associated with it which is controlled by a bit in this register. Accesses to each system memory window have the potential to occur with zero additional states which is also controlled by a bit in the register.

BIT POSITION	NAME	DESCRIPTION
7	Data Size	A "0" selects an 8-bit memory data path to the PC Card, and a "1" selects a 16-bit memory data path to the PC Card.
6	Zero wait State	If bit is set to "1", an 8-bit or 16-bit system memory accesses complete in 3 SYSCLKs or 2 SYSCLKs respectively, with internal ZEROWS# signal asserted to the PCI interfaces. If the bit is set to "0", the 8-bit or 16-bit memory access will complete in 6 SYSCLKs or 3 SYSCLKs with internal IOCHRDY asserted HIGH. If internal IOCHRDY becomes deasserted by internal wait state generation, or WAIT# signal, then setting this bit to "0" will cause 16-bit memory cycles to complete in more than 3 SYSCLKs. If internal IOCHRDY becomes deasserted by internal WAIT# signal, then setting this bit to "0" will cause 8-bit memory cycles to complete in more than 6 SYSCLKs. When the Zero wait State bit is set to "1" in the system Memory Address Mapping Start HIGH Byte Register, then the internal ZEROWS# output will be held HIGH for accesses to a 8-bit system memory window with both A0 and SBHE# equal to "0". **NOTE:** A logic LOW on IOCHRDY, either caused by an internal wait state generator or by WAIT# will force the ZEROWS# output HIGH.
[5:4]	Scratch Bits	These bits can be used for general purpose register storage and retrieval
[3:0]	Address [23:20]	System Memory Window start Address Start Address A23:A20 HIGH order address bits used to determine the start address of the corresponding system memory address mapping window.

SYSTEM MEMORY ADDRESS 0 MAPPING STOP LOW BYTE REGISTER (READ/WRITE)

Socket A: Index (Base + 12h)
Socket B: Index (Base + 52h)

These registers contain the low order address bits used to determine the stop address of the corresponding system memory address mapping window. This provides a minimum memory mapping window of 4 Kbytes.

BIT POSITION	NAME	DESCRIPTION
[7:0]	Address [19:12]	System Memory Window Stop Address A19:A12

SYSTEM MEMORY ADDRESS 0 MAPPING STOP HIGH BYTE REGISTER (READ/WRITE)

Socket A: Index (Base + 13h)
Socket B: Index (Base + 53h)

These registers contain the high order address bits used to determine the stop address of the corresponding system memory address mapping window. Each system memory window has the ability to extend a 16-bit system bus cycle by inserting wait states. Two bits in each of these register selects the number of wait states for a 16-bit access to the system memory window.

BIT POSITION	NAME	DESCRIPTION
[7 : 6]	Wait State(s) select bits[1:0]	These bits determine the number of additional wait states for a 16-bit access to the system memory window. The internal wait state generator will not cause additional wait states to be inserted for an 8-bit system access even if both bits are set to "1" because IOCHRDY will be pulled HIGH by the OZ6833 before the system samples IOCHRDY. If the PC Card supports the WAIT# signal, wait states will be generated by the PC Card asserting the WAIT# signal. Bit 6 and 5 should be set to "0" to disable the internal wait state generator from generating wait states.
		<table><tr><th>Wait State Bit 1</th><th>Wait State Bit 0</th><th>Number of Additional Wait States</th><th>of SYSCLKs per Access</th></tr><tr><td>0</td><td>0</td><td>Standard 16-bit Cycle</td><td>3</td></tr><tr><td>0</td><td>1</td><td>1</td><td>4</td></tr><tr><td>1</td><td>0</td><td>2</td><td>5</td></tr><tr><td>1</td><td>1</td><td>3</td><td>6</td></tr></table>
[5:4]	Reserved	
[3:0]	Address [23:20]	System Memory Window start Address Start Address A23:A20 HIGH order address bits used to determine the stop address of the corresponding system memory address mapping window.

CARD MEMORY OFFSET ADDRESS 0 LOW BYTE REGISTER (READ/WRITE)

Socket A: Index (Base + 14h)
Socket B: Index (Base + 54h)

These registers contain the low order address bits which are added to the system address bits **A19:A12** to generate the memory address for the PC card.

BIT POSITION	NAME	DESCRIPTION
[7:0]	Address [19:12]	Card Memory Offset Address A19:A12

CARD MEMORY OFFSET ADDRESS 0 HIGH BYTE REGISTER (READ/WRITE)

Socket A: Index (Base + 15h)
Socket B: Index (Base + 55h)

These registers contain the high order address bits which are added to the system address bits **A23:A20** to generate the memory address for the PC Card. The software write protect of the PC Card memory for the corresponding system memory window is controlled by this register. This register also controls if the corresponding system memory window is mapped to attribute or common memory on the PC Card.

BIT POSITION	NAME	DESCRIPTION
7	Write Protect	If bit is set to "1", write operations to the PC Card through the corresponding system memory window are inhibited. if bit is set to "0", write operations to the PC Card through the corresponding system memory window are allowed. WP Switch on the memory card alone will not block the memory write cycle, but only set the Memory Write Protect bit in the Interface Status register.
6	Reg Active	If bit is set to "1", accesses to the system memory window will result in attribute memory on the PC Card being accessed by asserting REG# to LOW. If bit is set to "0", accesses to the system memory will result in common memory on the PC card being accessed by driving REG# to HIGH.
[5:0]	Address [23:20]	Card Memory Offset Address A25:A20 Bits A25 and A24 will be added to the system address bits A23:A20 to generate the memory address for the PC Card.

CARD MEMORY ADDRESS 0 MAPPING START UPPER BYTE REGISTER (READ/WRITE)

Socket A: Index (Base + 17h)
Socket B: Index (Base + 57h)

These registers are used in comparing PCI address bit 31:24 for each R2 memory windows. It decides which 16-Mbyte page memory region in the 4Gbyte PCI address space.

BIT POSITION	NAME	DESCRIPTION
[7:0]	Address [31:24]	mapping start upper address byte A[31:24] are compared to PCI address.

SYSTEM MEMORY ADDRESSES 1-4 MAPPING REGISTERS (READ/WRITE)

System Memory Addresses 1-4 register functions duplicate Address 0. Below are the register addresses of each of the registers.

System Memory Address 1 Mapping Start Register LOW Byte

  Socket A: Index (Base + 18h)
  Socket B: Index (Base + 58h)

System Memory Address 1 Mapping Start Register HIGH Byte

  Socket A: Index (Base + 19h)
  Socket B: Index (Base + 59h)

System Memory Address 1 Mapping Stop Register LOW Byte

  Socket A: Index (Base + 1Ah)
  Socket B: Index (Base + 5Ah)

System Memory Address 1 Mapping Stop Register HIGH Byte

  Socket A: Index (Base + 1Bh)
  Socket B: Index (Base + 5Bh)

Card Memory Offset Address 1 LOW Byte

  Socket A: Index (Base + 1Ch)
  Socket B: Index (Base + 5Ch)

Card Memory Offset Address 1 HIGH Byte

  Socket A: Index (Base + 1Dh)
  Socket B: Index (Base + 5Dh)

System memory Address 1 Mapping Start Upper Byte

  Socket A: Index (Base + 1Fh)
  Socket B: Index (Base + 5Fh)

System Memory Address 2 Mapping Start Register LOW Byte

  Socket A: Index (Base + 20h)
  Socket B: Index (Base + 60h)

System Memory Address 2 Mapping Start Register HIGH Byte

  Socket A: Index (Base + 21h)
  Socket B: Index (Base + 61h)

System Memory Address 2 Mapping Stop Register LOW Byte

  Socket A: Index (Base + 22h)
  Socket B: Index (Base + 62h)

System Memory Address 2 Mapping Stop Register HIGH Byte

  Socket A: Index (Base + 23h)
  Socket B: Index (Base + 63h)

Card Memory Offset Address 2 LOW Byte

  Socket A: Index (Base + 24h)
  Socket B: Index (Base + 64h)

Card Memory Offset Address 2 HIGH Byte

  Socket A: Index (Base + 25h)
  Socket B: Index (Base + 65h)

System memory Address 2 Mapping Start Upper Byte

  Socket A: Index (Base + 27h)
  Socket B: Index (Base + 67h)

System Memory Address 3 Mapping Start Register LOW Byte

Socket A: Index (Base + 28h)
Socket B: Index (Base + 68h)

System Memory Address 3 Mapping Start Register HIGH Byte

Socket A: Index (Base + 29h)
Socket B: Index (Base + 69h)

System Memory Address 3 Mapping Stop Register LOW Byte

Socket A: Index (Base + 2Ah)
Socket B: Index (Base + 6Ah)

System Memory Address 3 Mapping Stop Register HIGH Byte

Socket A: Index (Base + 2Bh)
Socket B: Index (Base + 6Bh)

Card Memory Offset Address 3 LOW Byte

Socket A: Index (Base + 2Ch)
Socket B: Index (Base + 6Ch)

Card Memory Offset Address 3 HIGH Byte

Socket A: Index (Base + 2Dh)
Socket B: Index (Base + 6Dh)

System memory Address 3 Mapping Start Upper Byte

Socket A: Index (Base + 2Fh)
Socket B: Index (Base + 6Fh)

System Memory Address 4 Mapping Start Register LOW Byte

Socket A: Index (Base + 30h)
Socket B: Index (Base + 70h)

System Memory Address 4 Mapping Start Register HIGH Byte

Socket A: Index (Base + 31h)
Socket B: Index (Base + 71h)

System Memory Address 4 Mapping Stop Register LOW Byte

Socket A: Index (Base + 32h)
Socket B: Index (Base + 72h)

System Memory Address 4 Mapping Stop Register HIGH Byte

Socket A: Index (Base + 33h)
Socket B: Index (Base + 73h)

Card Memory Offset Address 4 LOW Byte

Socket A: Index (Base + 34h)
Socket B: Index (Base + 74h)

Card Memory Offset Address 4 HIGH Byte

Socket A: Index (Base + 35h)
Socket B: Index (Base + 75h)

System memory Address 4 Mapping Start Upper Byte

Socket A: Index (Base + 3Fh)
Socket B: Index (Base + 7Fh)

The O₂Micro Mode

O₂MICRO MODE CONTROL A REGISTER (READ/WRITE)

Socket A: Index (Base + 38h)
Socket B: Index (Base + 78h)

During power-on reset or hardware reset, bit 6 is loaded with value of pin 131 (SDATA/SMBDATA), and bit 5 is loaded with value of pin 130 (SLATCH/SMBCLK). These values can be preset using pull-down and pull-up resistors

BIT POSITION	NAME	DESCRIPTION
7	Reserved	
[6:5]	Pwrchip	**00 => Reserved** **01 => parallel socket pwr** **10 => TI TPS2202IDF** **11 => SMBUS MAX1601**
[4:0]	Reserved	

O₂MICRO MODE CONTROL B REGISTER (READ/WRITE)

Socket A: Index (Base + 39h)
Socket B: Index (Base + 79h)

This register contains Chip ID setting, which directly load the Intel365SL B step or C step or O₂Micro mode software driver.

7	RI_OUT Enable	**"0"** : Indicates to disable the output for pin RI_OUT. **"1"**: Indicates to enable the output for pin RI_OUT.
6 -4	Reserved	This bit is reserved.
3	VS2#	This bit is connected to PCMCIA pin 57. Cards that will only operate at 3.3V will drive this pin to a "0". Note that this bit is provided for possible future PCMCIA specifications. **"0"** : 3.3V card detected. **"1"** : Old or 5V card detected.
2	5V Detect (VS1#)	This bit is connected to PCMCIA pin 34. Cards that will only operate at 3.3V will drive this pin to a "0". Note that this bit is provided for possible future PCMCIA specifications. **"0"** : 3.3V card detected. **"1"** : Old or 5V card detected.

[1:0]	Chip ID parameter	These bits set the Chip ID, index 00h/40h, Read only register setting:
		
		Bit 1 Bit 0 Chip ID
		  1 1 Reserved (Default)
		  1 0 O₂Micro Mode
		  0 1 Intel365SL C Step
		  0 0 Intel365SL B Step

O₂MICRO MODE CONTROL C REGISTER (READ/WRITE)

Socket A: Index (Base + 3Ah)
Socket B: Index (Base + 7Ah)

BIT POSITION	NAME	DESCRIPTION
[7:4]	Reserved	
[3]	Zvideo	"0" : socket address lines are normal "1" : socket address lines A[25:4] are HIGH-Impedance
[1:0]	DREQ Select/Enable	00 : Disable 01 : INPACK# 10 : WP/IOIS16 11 : BVD2/SPKR#

O₂MICRO MODE CONTROL D REGISTER (READ/WRITE)

Socket A: Index (Base + 3Bh)
Socket B: Index (Base + 7Bh)

During power-on reset or hardware reset, bit 1 is loaded with value of pin 133 (LED_OUT), and bit 0 is loaded with value of pin 128 (SPKR_OUT). These values can be preset using pull-down and pull-up resistors.

BIT POSITION	NAME	DESCRIPTION
7-4	Reserved	Read as "0100"
3	CardBus Clkrun# enable	Bit is "1", indicates Clkrun# support enabled on PCI Bus. Bit is "0", indicates Clkrun# support disabled on PCI Bus (Default).
2	PCI Clkrun# enable	Bit is "1", indicates Clkrun# support enabled on PCI Bus. Bit is "0", indicates Clkrun# support disabled on PCI Bus (Default).
1-0	System Interrupt Mode	These bits indicate the type of interrupt mode selected in PCI-Compatible interrupt mode 00=> PC/PCI interrupt mode 01=> Reserved 10=> PCI/Way interrupt mode 11=> PCI interrupt mode (Default)

MHPG DMA REGISTER (READ/WRITE)

Socket A: Index (Base + 3Ch)
Socket B: Index (Base + 7Ch)

BIT POSITION	NAME	DESCRIPTION
[7:5]	Reserved	Read as "000"
4	Status Change Interrupt Enable	bit is "0" indicates that when Socket Status changes will **not** generate the Interrupt bit is "1" indicates that when Socket Status changes will generate the Interrupt **(Default)**
3	CINT# Enable	bit is "0" indicates that when CardBus CINT# active will **not** generate the Interrupt bit is "1" indicates that when CardBus CINT# active will generate the Interrupt **(Default)**
2-0	MHPG DMA Channel #	Define the DMA channel number from 0h-7h

FIFO ENABLE REGISTER (READ/WRITE)

Socket A: Index (Base + 3Dh) This register bits are shared by Socket A and B
Socket B: Index (Base + 7Dh)

BIT POSITION	NAME	DESCRIPTION
7	Buffer Enable	bit is "0" indicates that CardBus bridge memory FIFO full buffer disabled bit is "1" indicates that CardBus bridge memory FIFO full buffer enabled
6	MEM_POSTWR	bit is "0" indicates that Cardbus bridge memory post write function disabled bit is "1" indicates that Cardbus bridge memory post write function enabled
5	Reserved	
4	PCI_FIFO	bit is "1", indicates PCI side Dword buffer enabled bit is "0", indicates PCI side Dword buffer disabled
[3:0]	Reserved	

O2 MODE CONTROL REGISTER E (READ/WRITE)

Socket A: Index (Base + 3Eh). This register bits are shared by Socket A and B.
Socket B: Index (Base + 7Eh)

BIT POSITION	NAME	DESCRIPTION
[7:5]	Reserved	
4	SKTA_ACTV	bit is "0" indicates LED_OUT/SKT_ACTV pin is Led_Out bit is "1" indicates LED_OUT/SKT_ACTV pin is SocketA_Activity
3	LED_OUT Enable	"1" indicates that enable the output for pin LED_OUT(**Default)** "0" indicates that disable the output for pin LED_OUT
2	Reserved	
1	SPKR_OUT Enable	"1" indicates that enable the output for pin SPKR_OUT**(Default)** "0" indicates that disable the output for pin SPKR_OUT
0	MHPG DMA MODE	"0" indicates that MHPG DMA Mode not enabled. "1" indicates that MHPG DMA MODE Enabled

DC CHARACTERISTICS

DC Table for Vcc = 4.5V to 5.5V

Symbol	Parameter	Min	Max	Units
V_{CC}	Power Supply Voltage	4.5	5.5	
V_{IH}	Input HIGH Voltage	2.0	V_{CC} + 0.3	V
V_{II}	Input LOW Voltage	-0.3	0.8	V
V_{OH}	Output HIGH Voltage	2.4		V
V_{OL}	Output LOW Voltage		0.4	V
I_{IL}	Maximum Input Leakage Current		+/- 10	uA
I_{OL}	Maximum Output Leakage		+/- 10	uA
I_{CC}	Supply Current		50	mA
I_{CC1}	Supply Current / Power Down Mode [Outputs Tri-stated, Internal Clock stop]	35	-	uA

DC Table for Vcc = 3.0V to 3.6V

Symbol	Parameter	Min	Max	Units
V_{CC}	Power Supply Voltage	3.0	3.6	
V_{IH}	Input HIGH Voltage	2.0	V_{CC} + 0.3	V
V_{Il}	Input LOW Voltage	-0.3	0.8	V
V_{OH}	Output HIGH Voltage	2.4		V
V_{OL}	Output LOW Voltage		0.4	V
I_{IL}	Maximum Input Leakage Current		+/- 10	uA
I_{OL}	Maximum Output Leakage		+/- 10	uA
I_{CC}	Supply Current		30	mA
I_{CC1}	Supply Current / Power Down Mode [Outputs Tri-stated, Internal Clock stop]	20	-	uA

Capacitance

Symbol	Parameter	0 Degree C to 70 Degree C	Units
C_{IN}	Maximum Input Capacitance	10	pF
C_{OUT}	Maximum Output Capacitance	10	pF
C_{IO}	Maximum I/O Capacitance	10	pF

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	DC Power Supply Voltage	-0.5 to + 7.0	V
V_{IN}, V_{OUT}	DC Input, Output Voltage	-0.5 to V_{DD} + 0.5	V
I	DC Current Drain V_{DD} and V_{SS} Pins	100	mA
T_{STG}	Storage Temperature	-55 to +150	Degree C
T_L	Lead Temperature	250	Degree C
$T_{OPER|}$	Operation Temperature	0 to +70	Degree C

AC CHARACTERISTICS
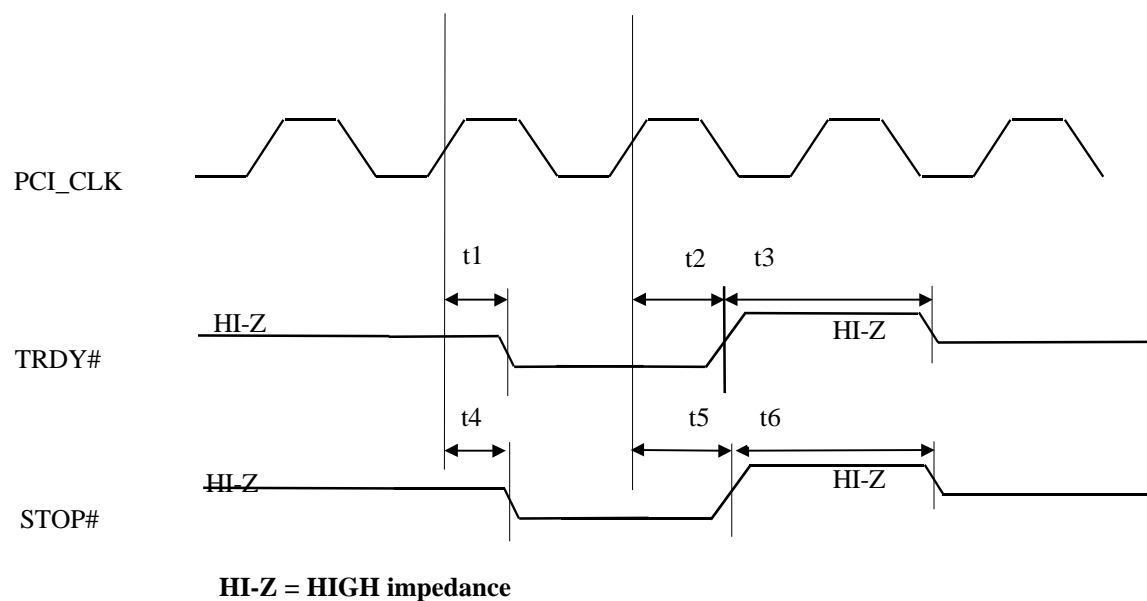
PCI Bus Timing

HI-Z = HIGH impedance
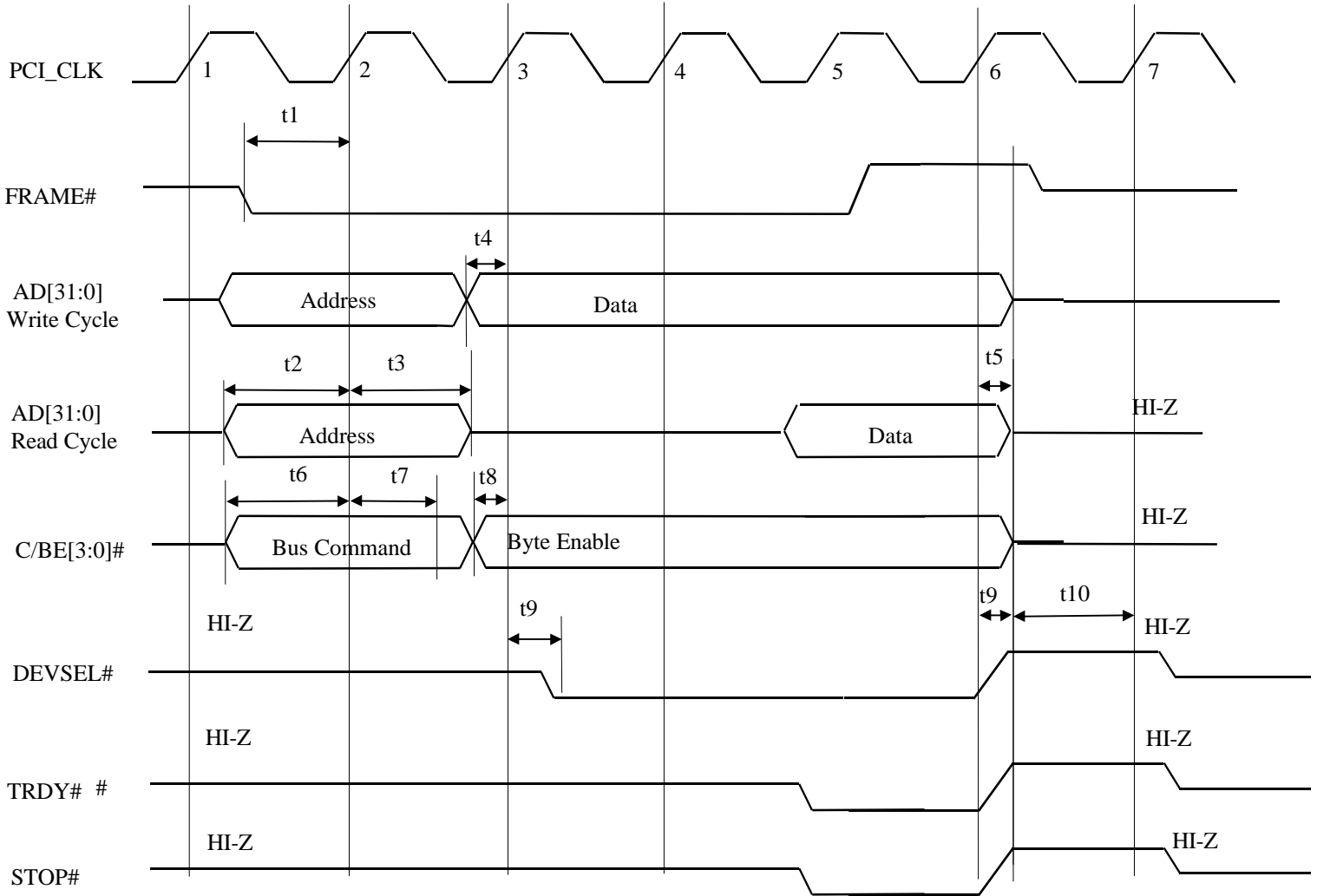
**FRAME#, AD[31:0], C/BE[3:0]#, DEVSEL#, TRDY# and STOP#
(PCI Bus)**

TRDY#,STOP# Timing

Symbol	Parameter	MIN	MAX	MIN	MAX	Units
t1	TRDY# active delay from PCI_CLK	-	11	-	11	ns
t2	TRDY# inactive delay from PCI_CLK	-	11	-	11	ns
t3	TRDY# HIGH before HI-Z	1	-	1	-	PCI_CLK
t4	STOP# active delay from PCI_CLK	-	11	-	11	ns
t5	STOP# inactive delay from PCI_CLK	-	11	-	11	ns
t6	STOP# HIGH before HI-Z	1	-	1	-	PCI_CLK

HI-Z = HIGH impedance

TRDY# and STOP# Delay (PCI Bus)

O₂Micro
2901 Tasman Drive, Ste. 205
Santa Clara, CA 95054   Page 57
Tel: (408) 987-5920
Fax: (408) 987-5929
©OZ6833-DS-1.2

IDSEL Timing in a Configuration Cycle

Symbol	Parameter	MIN	MAX	Units
t1	IDSEL setup to PCI_CLK	7	-	ns
t2	IDSEL hold from PCI_CLK	0	-	ns
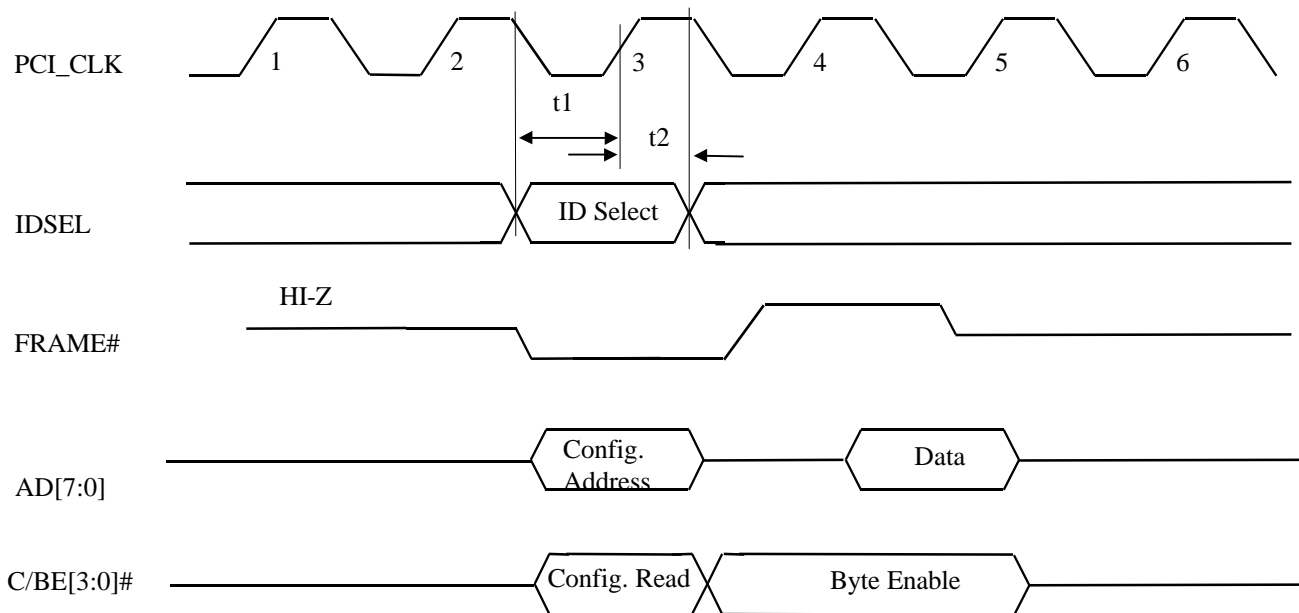
HI-Z = HIGH impedance

IDSEL Timing in a Configuration Cycle (PCI Bus)

PAR Timing

Symbol	Parameter	MIN	MAX	Units
t1	PAR setup to PCI_CLK (input to CL-PD6730)	7	-	ns
t2	PAR hold from PCI_CLK (input to OZ6833)	0	-	ns
t3	PAR valid delay from PCI_CLK (output from OZ6833)	-	11	ns
t4	PAR hold from PCI_CLK (output from OZ6833)	0	-	ns
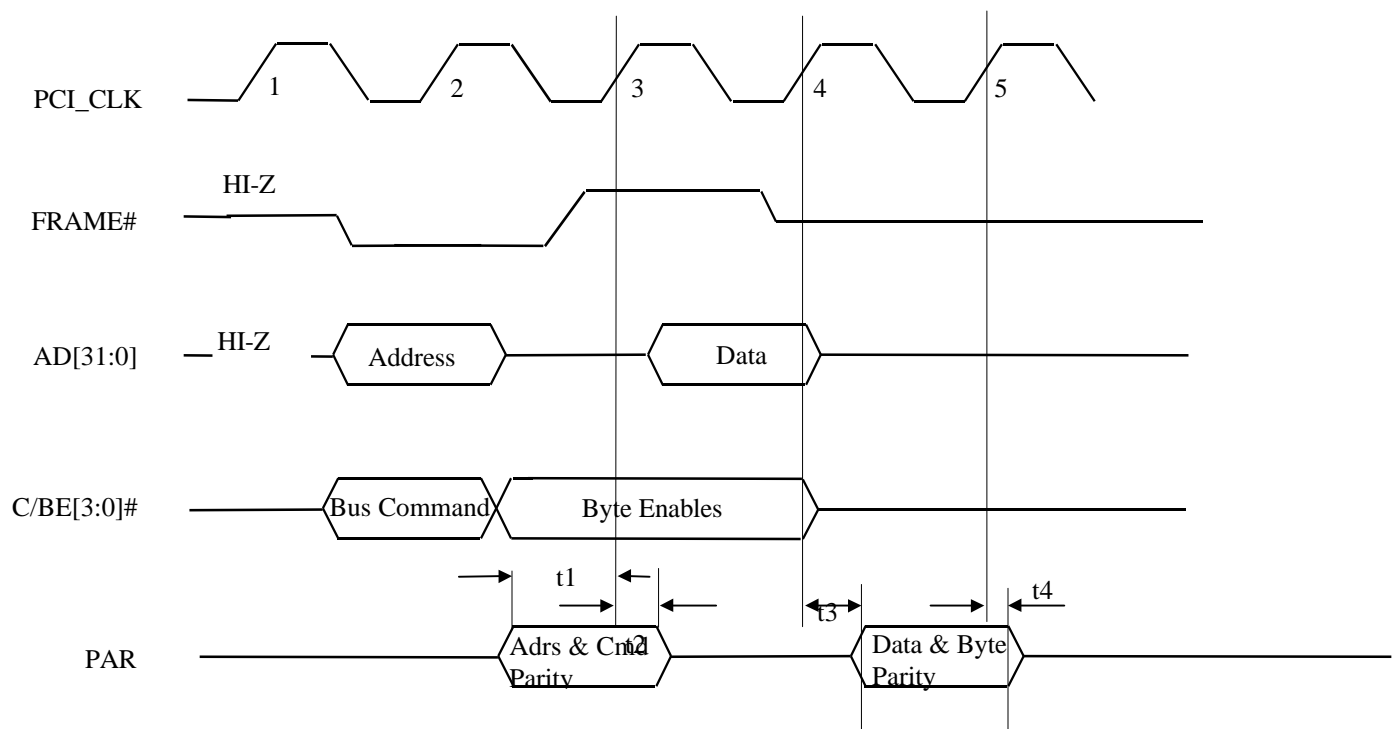
PAR goes HIGH or LOW depending on AD[31:0] and C/BE[3:0]# values.

PAR Timing (PCI Bus)

System Interrupt Timing

Pulse Mode Interrupt Timing

Symbol	Parameter	MIN	MAX	Units
t1	IRQ[XX] LOW or HIGH	16	16	PCI_CLK

IRQ[XX]   HI-Z   HI-Z

                                        t1   t1
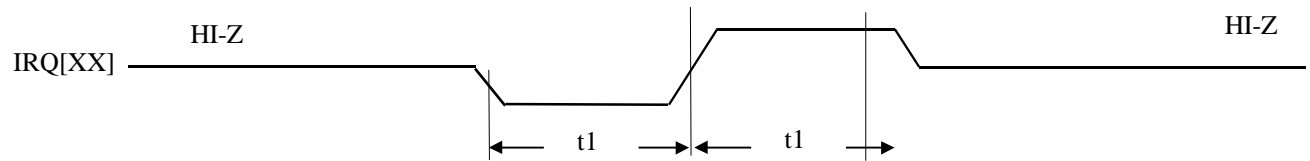
HI-Z = HIGH impedance

Pulse Mode Interrupt Timing

I/O Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t1	REG# or Address setup to Command active	70		ns
t2	Command pulse width	165		ns
t3	Address hold and Write Data valid from Command inactive	20		ns
t4	Card IOCS16# delay from valid Address(PC Card specification)		35	ns
t5	Data setup before IORD# inactive	60		ns
t6	Data hold after IORD# inactive	0		ns
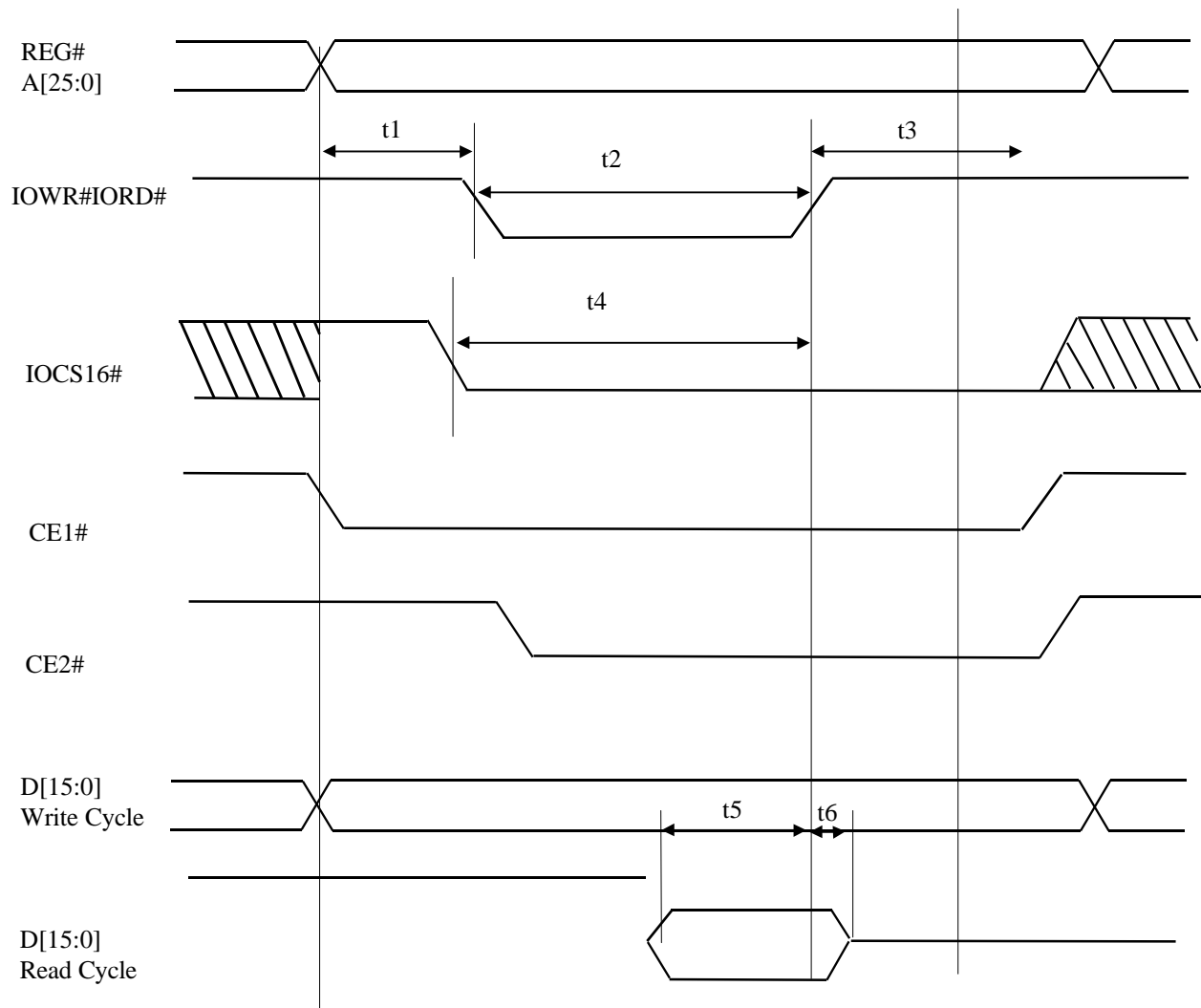
Memory I/O Read/Write Timing

PC Card Bus Timing

Memory Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t1	REG#, CE[2:1]#; Address, and Write Data setup to Command active	30		ns
t2	Command pulse width	150		ns
t3	Address hold and Write Data valid from Command inactive	20		ns
t4	WAIT# active from Command active		35	ns
t5	Command hold from WAIT# inactive	0		ns
t6	Data setup before OE# inactive	80		ns
t7	Data hold after OE# inactive	30		ns

Memory Read/Write Timing

©OZ6833-DS-1.2
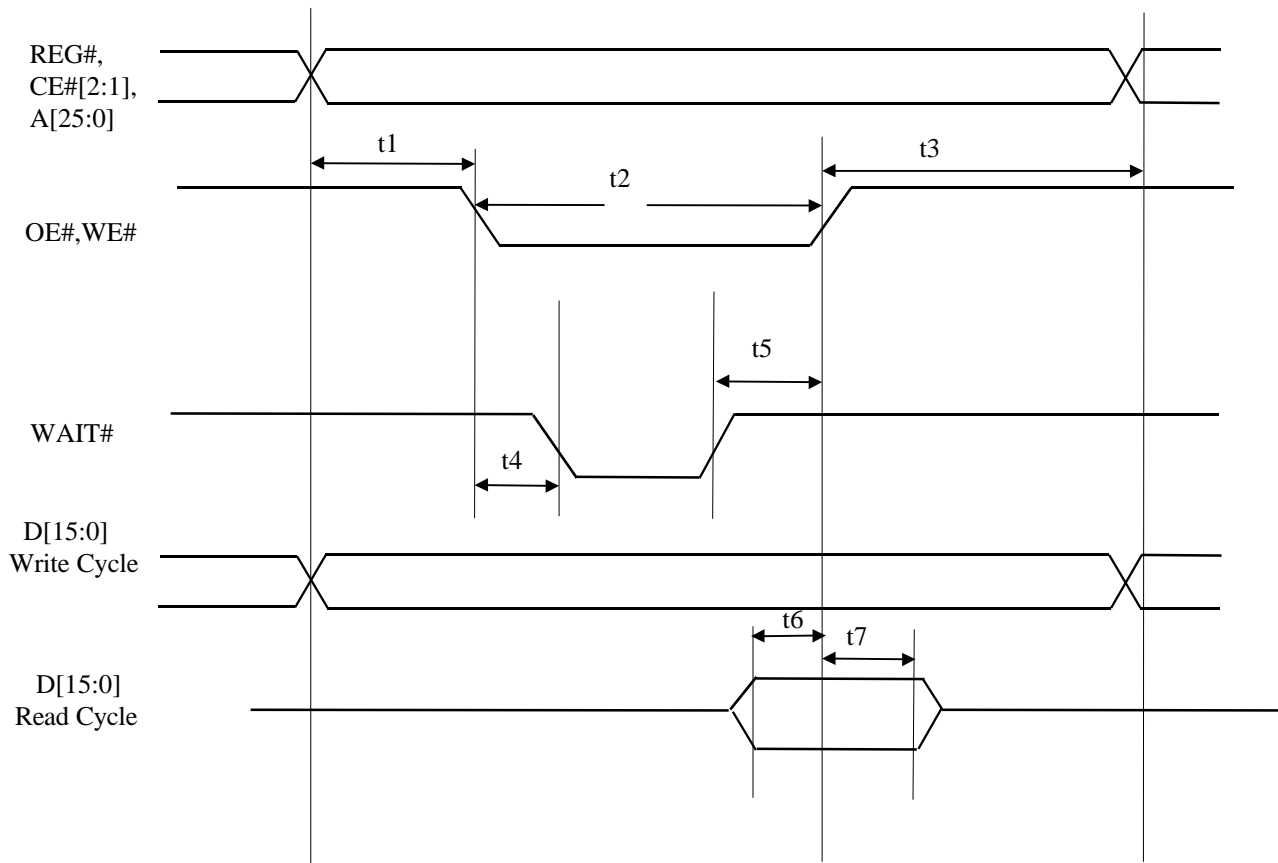
Normal Byte Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t1	Address setup to Command active	70		ns
t2	Command pulse width	165		ns
t3	Address hold from Command inactive	20		ns
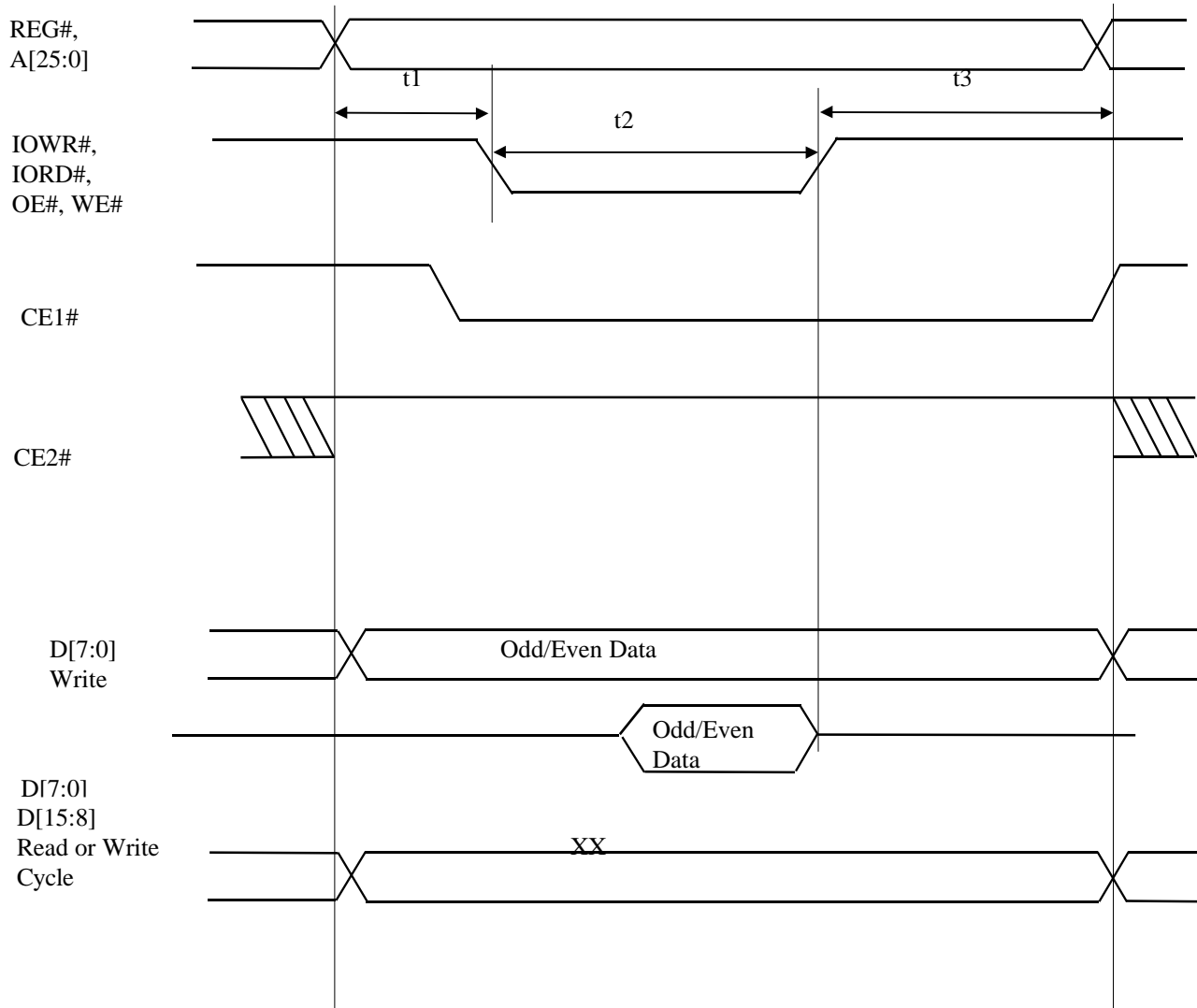
Normal Byte Read/Write Timing

PC Card Read/Write Timing when System is 8-Bit

Symbol	Parameter	MIN	MAX	Units
t1	REG# or Address setup to Command active	70		ns
t2	Command pulse width	165		ns
t3	Address hold from Command inactive	20		ns
t4	Data setup before Command inactive	60		ns
t5	Data hold after command inactive	0		ns
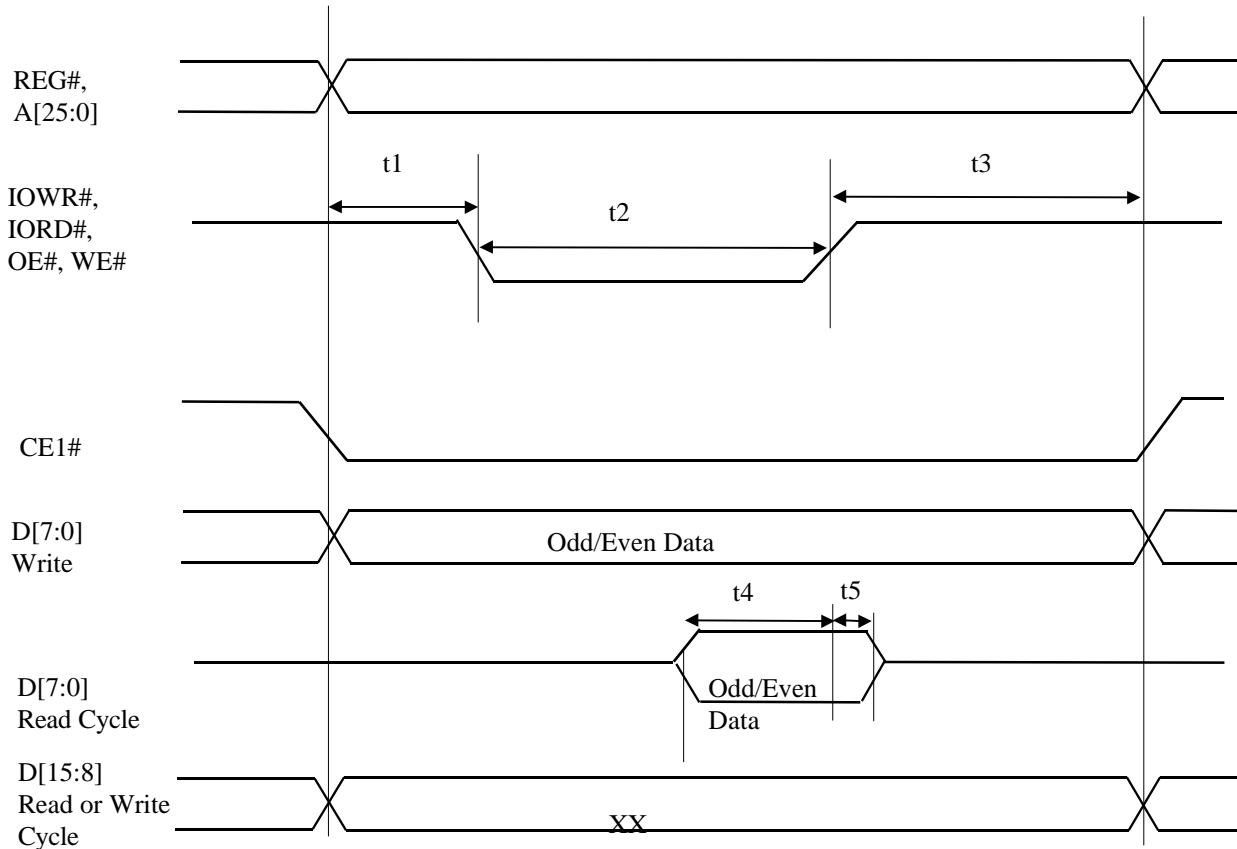
**PC Card Read/Write Timing when System is 8 Bit
(SBHE Tied HIGH)**

16-Bit System to 8-Bit I/O Card: Odd Byte Timing

Symbol	Parameter	MIN	MAX	Units
t1	IOIS16# inactive to CE2# inactive		20	ns
t2	IOIS16# inactive to CE1# active		20	ns
t3	Address setup to Command active	70		ns
t4	Command pulse width	165		ns
t5	Address hold from Command inactive	20		ns
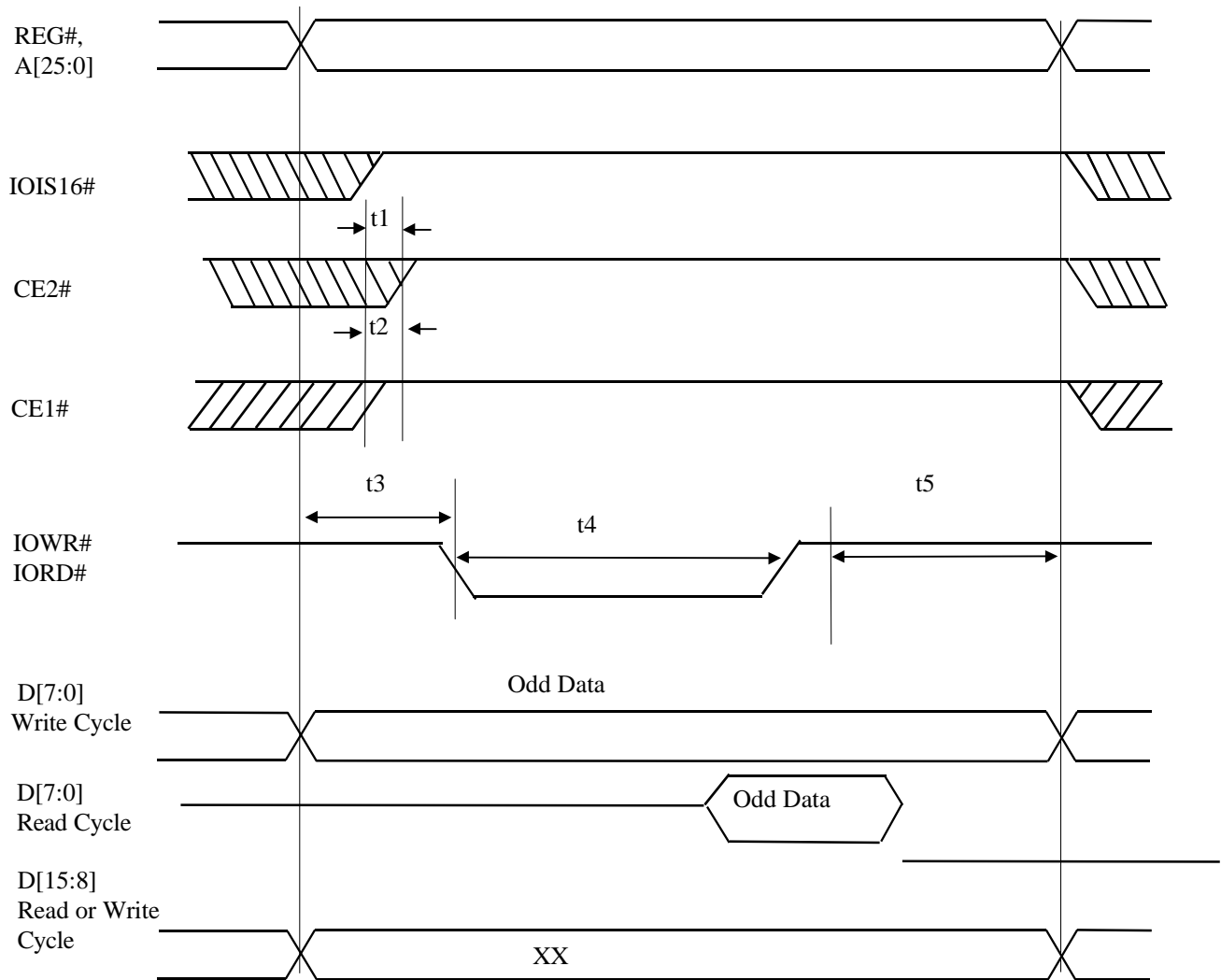
16-Bit System to 8-Bit I/O Card: Odd Byte Timing

Package Specifications
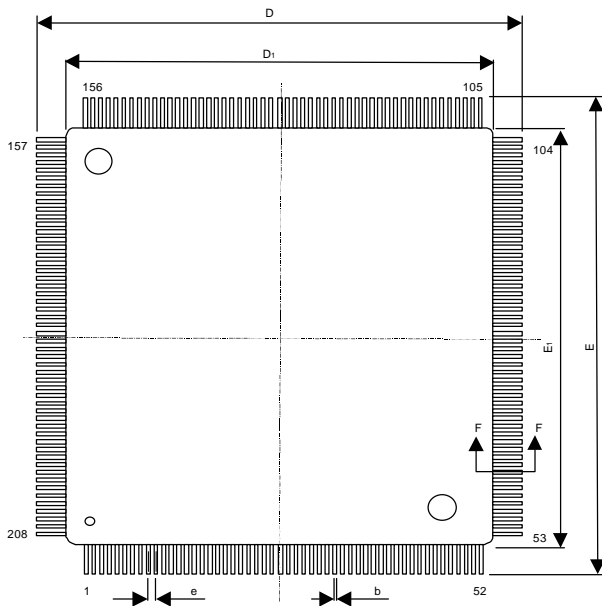
Symbol	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.063	-	-	1.60
A$_1$	0.002	-	0.006	0.05	-	0.15
A$_2$	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	-	0.008	0.09	-	0.20
D	1.181			30.00 BSC.		
D$_1$	1.102			28.00 BSC.		
E	1.181			30.00 BSC.		
E$_1$	1.102			28.00 BSC.		
e	0.020 BSC.			0.50 BSC.		
L	0.018	0.024	0.030	0.45	0.60	0.75
L$_1$	0.039 REF			1.00 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

SEATING PLANE

WITH PLATING

BASE METAL

SEC: B-B

GAGE PLANE

SEC: F-F

0.25
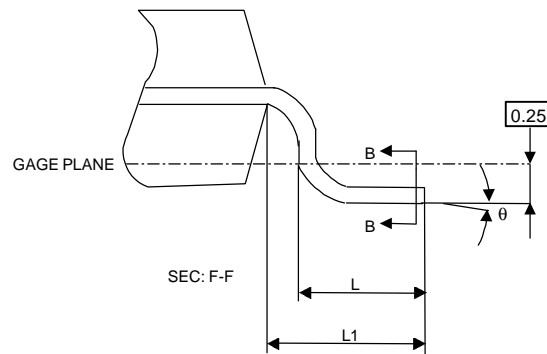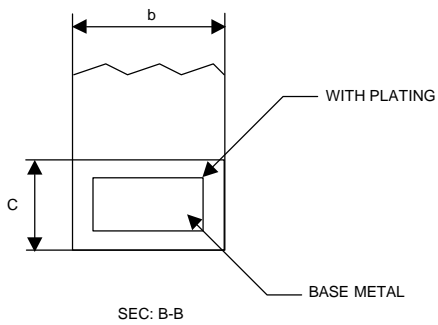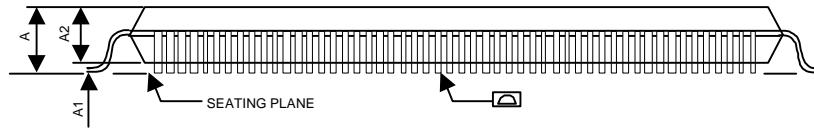
OZ6833 208-PIN TQFP

O2MICRO, INC.